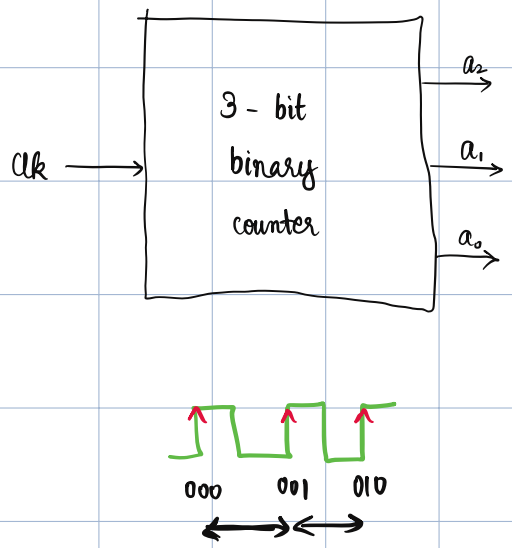
18 Nov 2024 – Digital Circuits – Week 16

Delay same → a_0, a_1, a_2

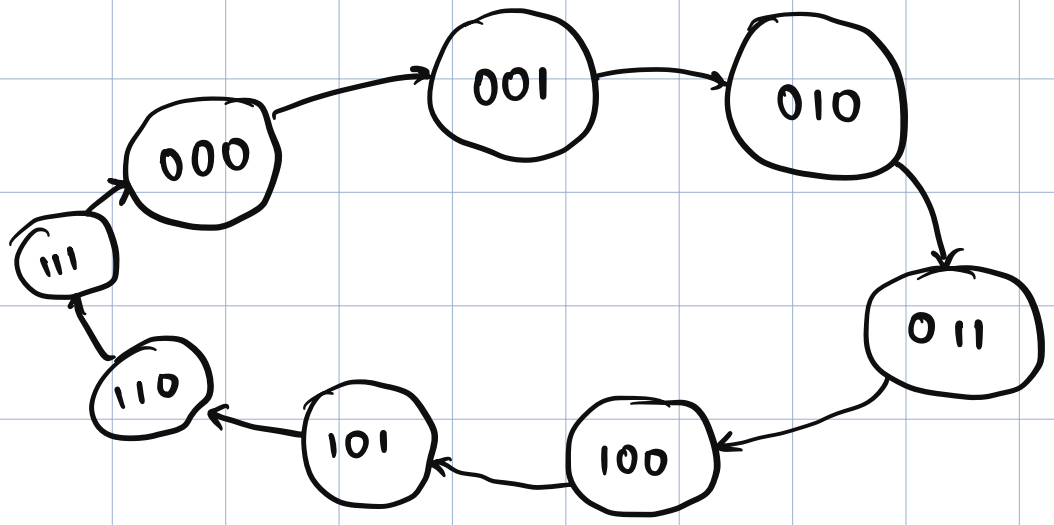
but don't change together } after output of 1st, 2nd gets its input



State table

	Present state			Next state		
	a_2	a_1	a_0	a_2^F	a_1^F	a_0^F
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	1	1
3	0	1	1	1	0	0
4	1	0	0	1	0	1
5	1	0	1	1	1	0
6	1	1	0	1	1	1
7	1	1	1	0	0	0

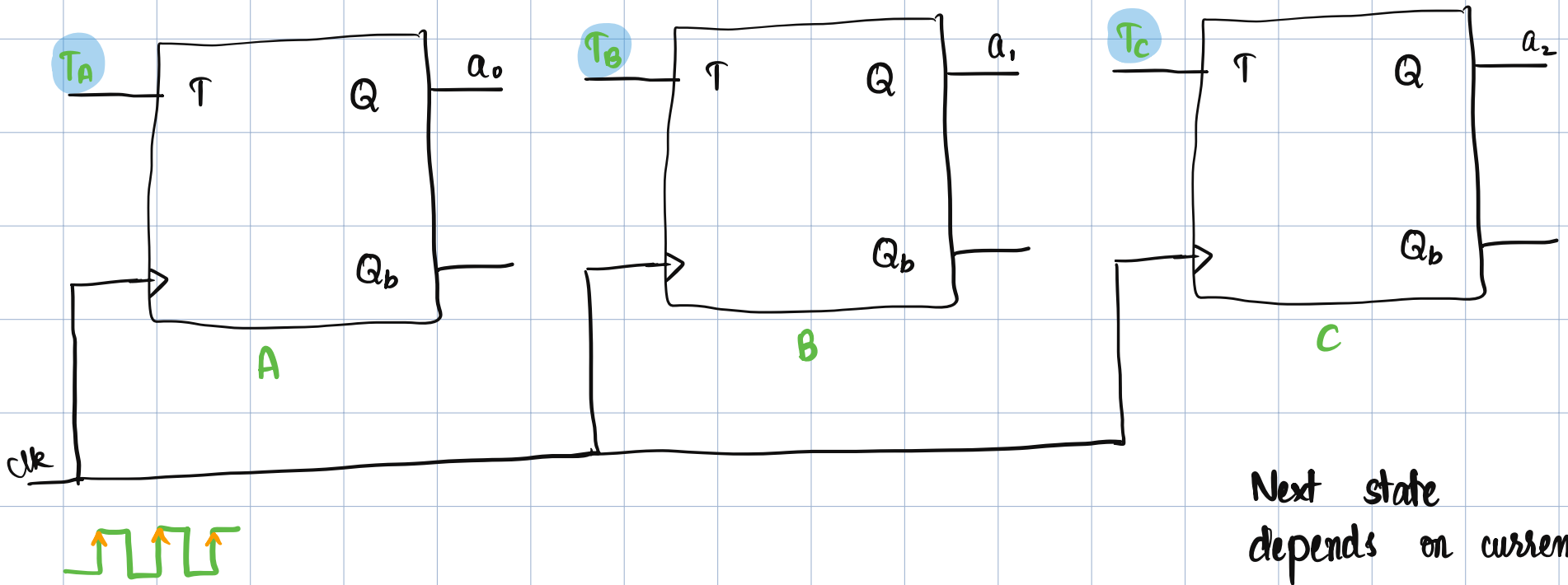
→ 8 states



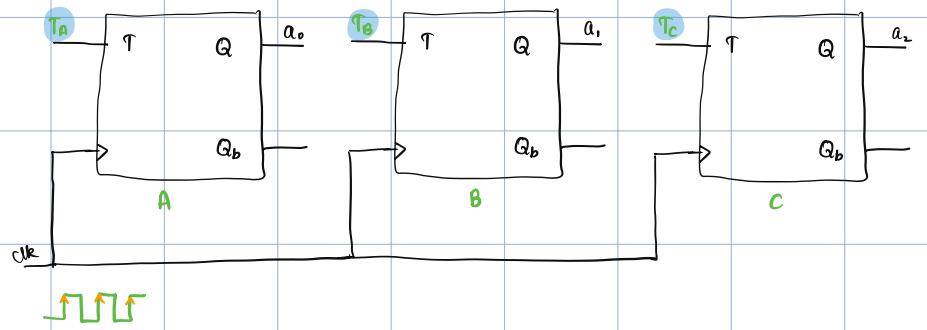
State diagram

* 3 flip-flops are needed to store 8 states
* Any of the flip-flops topology can be chosen → this will decide the complexity of the associated combinational circuit.

Choosing T - FF for 3 bit counter : (Synchronous)



Next state depends on current state



State table

	Present state			Next state					
	a_2	a_1	a_0	a_2^F	a_1^F	a_0^F	T_C	T_B	T_A
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	1	1	0	0	1	1
6	1	1	0	1	1	1	0	0	1
7	1	1	1	0	0	0	1	1	1

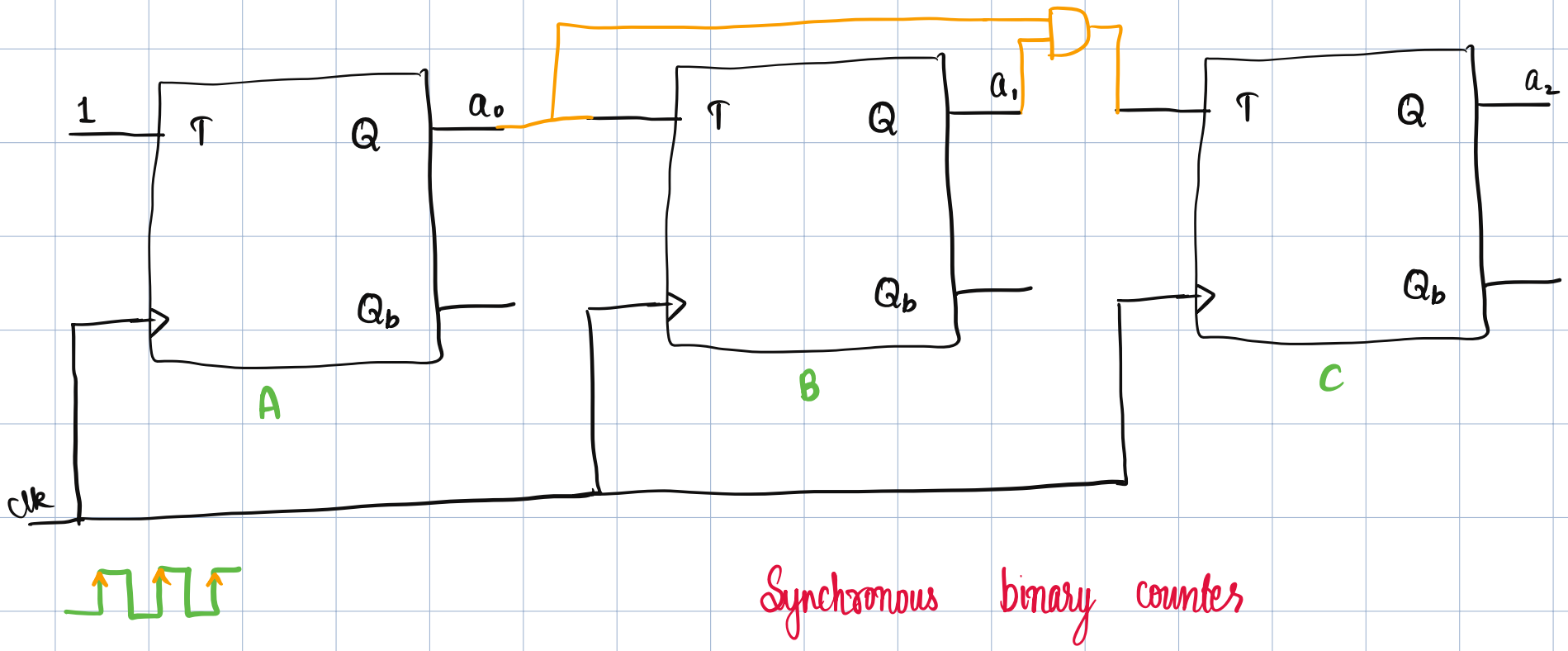
→ 8 states

should be set before clock edge → entries change, if D-flip-flop is used

$$T_A = f_1(a_2, a_1, a_0) = 1$$

$$T_B = f_2(a_2, a_1, a_0) = a_0$$

$$T_C = f_3(a_2, a_1, a_0) = a_1 \cdot a_0$$



Synchronous binary counter

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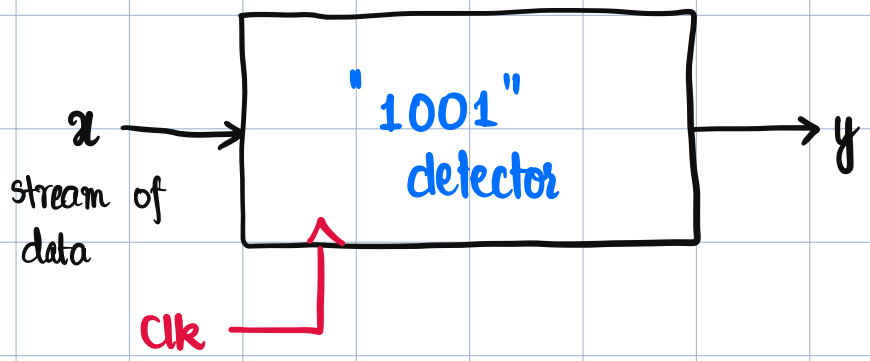
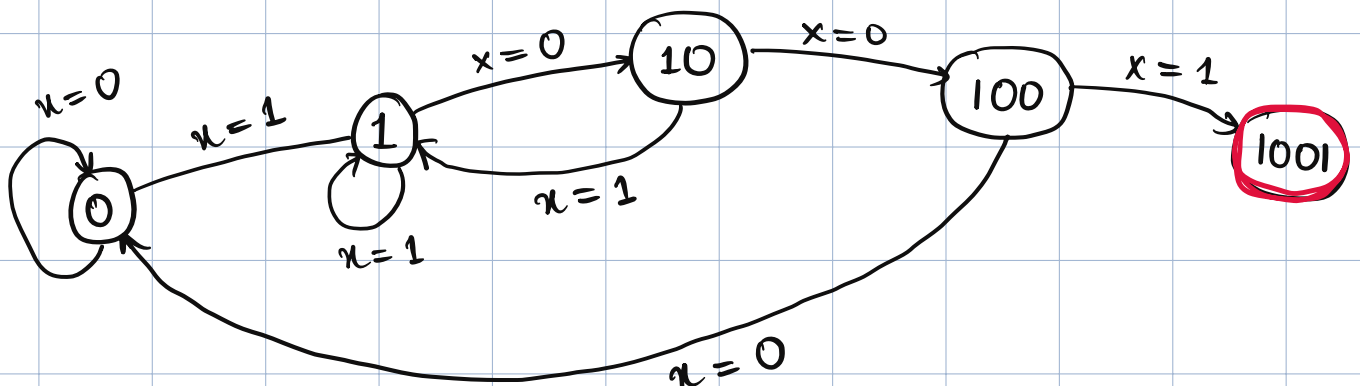
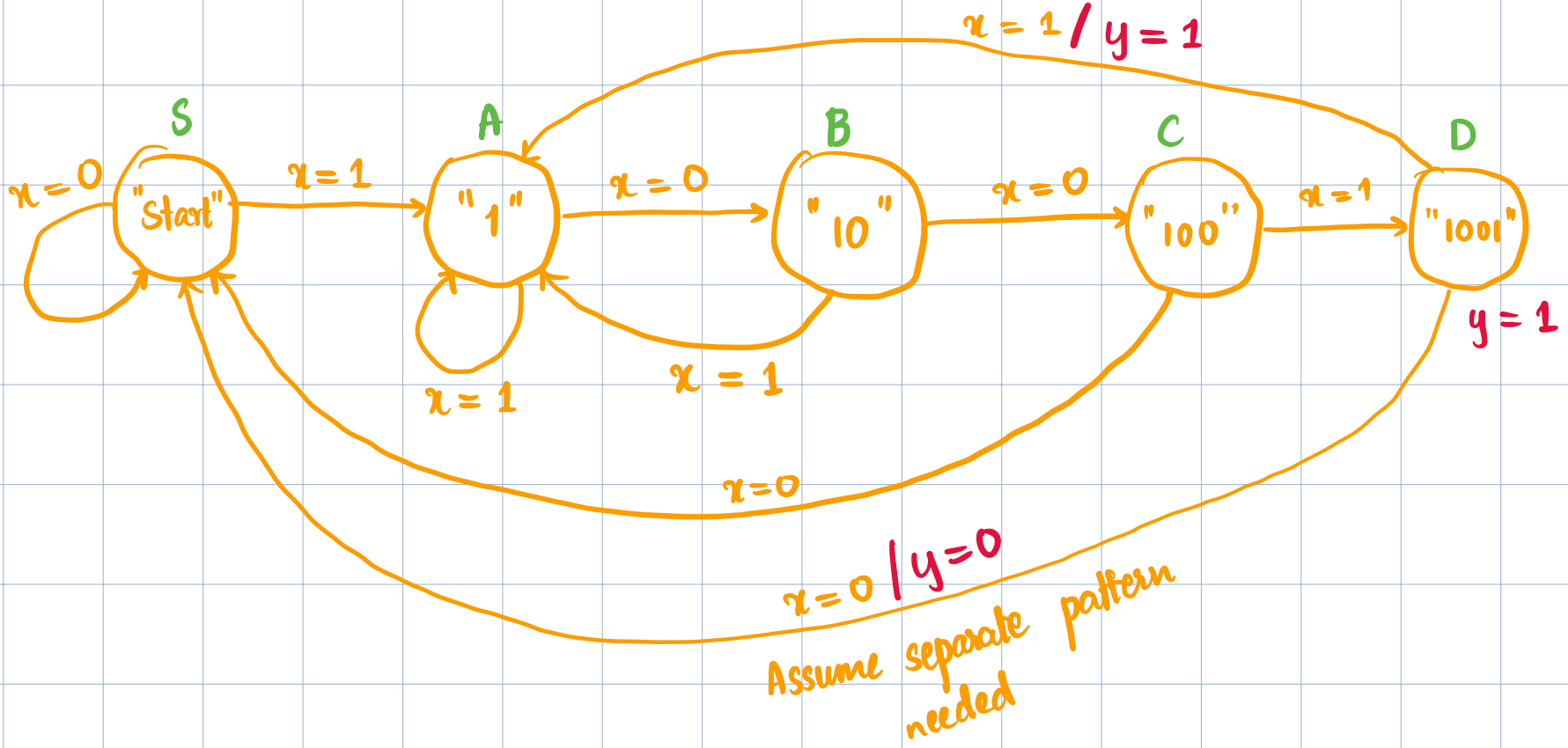
recognizing patterns

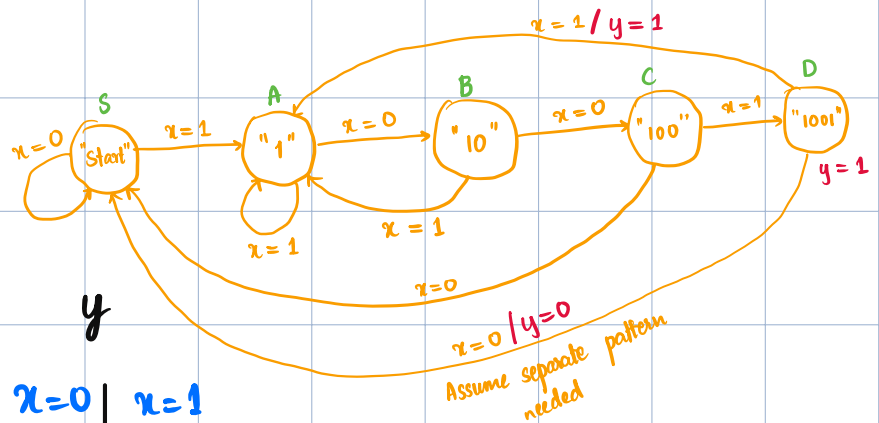
Ex:



1 0 0 1 1 1 0 0 1 0 1 1 1




S
A
B
C
D
"Start"
"1"
"10"
"100"
"1001"
x = 0
x = 1
x = 0
x = 0
x = 1
x = 1
x = 1 / y = 1
x = 1
x = 0
x = 0 / y = 0
y = 1
Assume separate pattern needed

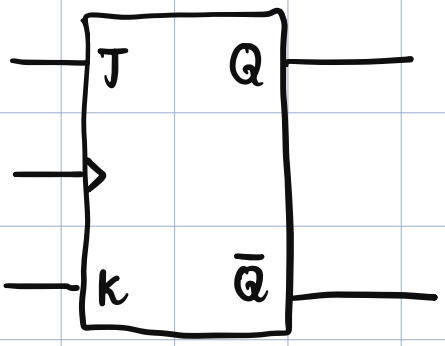


Present state	Next state $x=0$	Next state $x=1$	y $x=0$	y $x=1$
S	S	A	0	0
A	B	A	0	0
B	C	A	0	0
C	S	D	0	0
D	S	A	1	1

← No redundant states

5 states → 3 flip-flops

* Choosing 3 J-K flip-flop for the implementation.



Characteristic table of J-K flipflop

J	K	Q^f
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

Q^f → Next o/p

Q → present o/p

$$Q^F = f(Q, J, K)$$

$$= \bar{Q}J + Q\cdot\bar{K}$$

Excitation eqn

Q	Q^F	J	K
0	0	0	0/1 ×
0	1	1	1/0 ×
1	0	1/0 ×	1
1	1	1/0 ×	0

Excitation table

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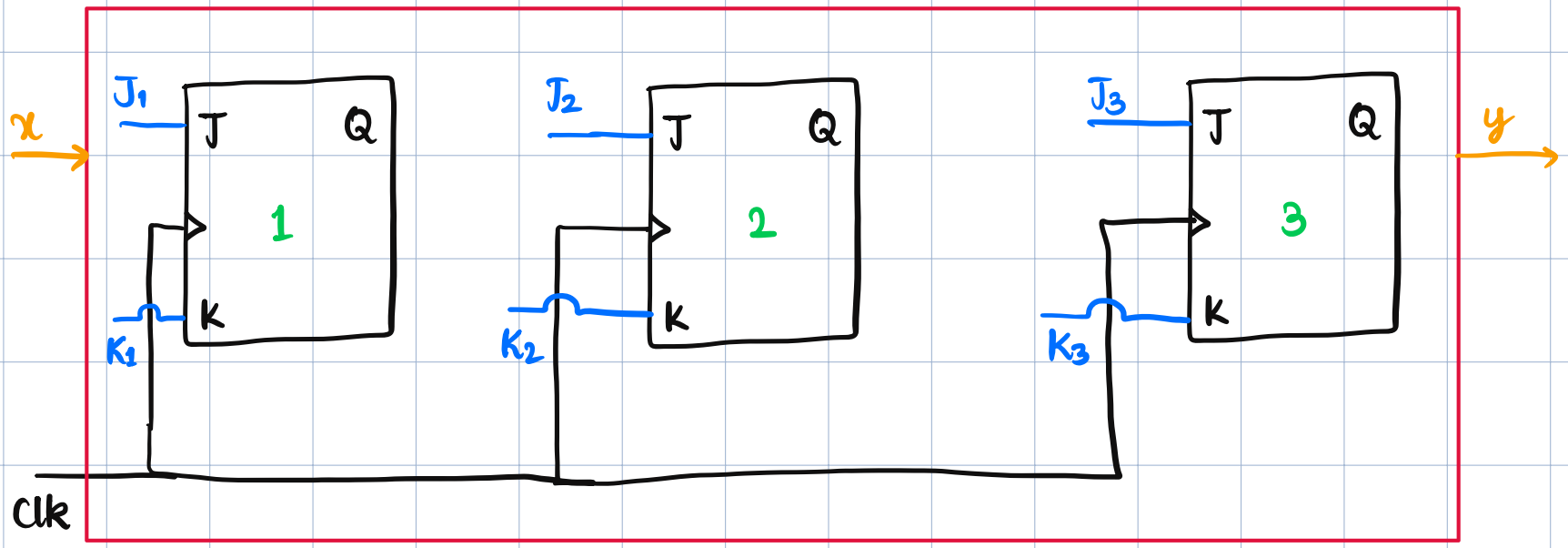
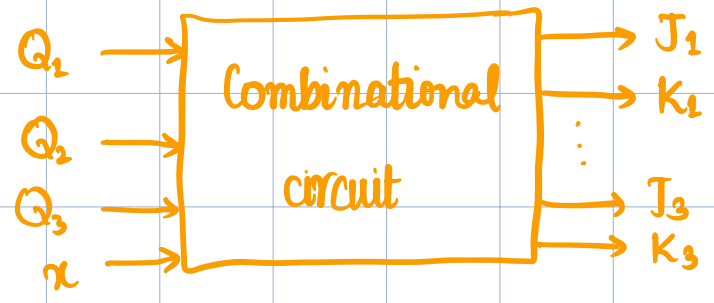


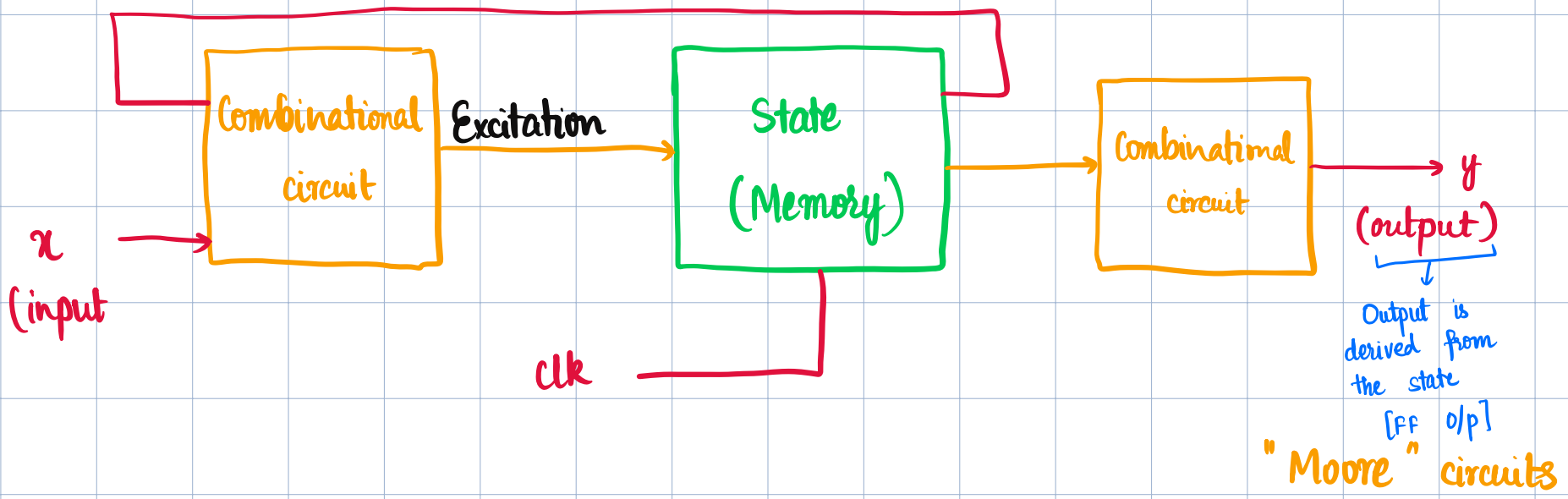
Present state	Next state x=0	Next state x=1	y x=0	y x=1
S	S	A	0	0
A	B	A	0	0
B	C	A	0	0
C	S	D	0	0
D	S	A	1	1

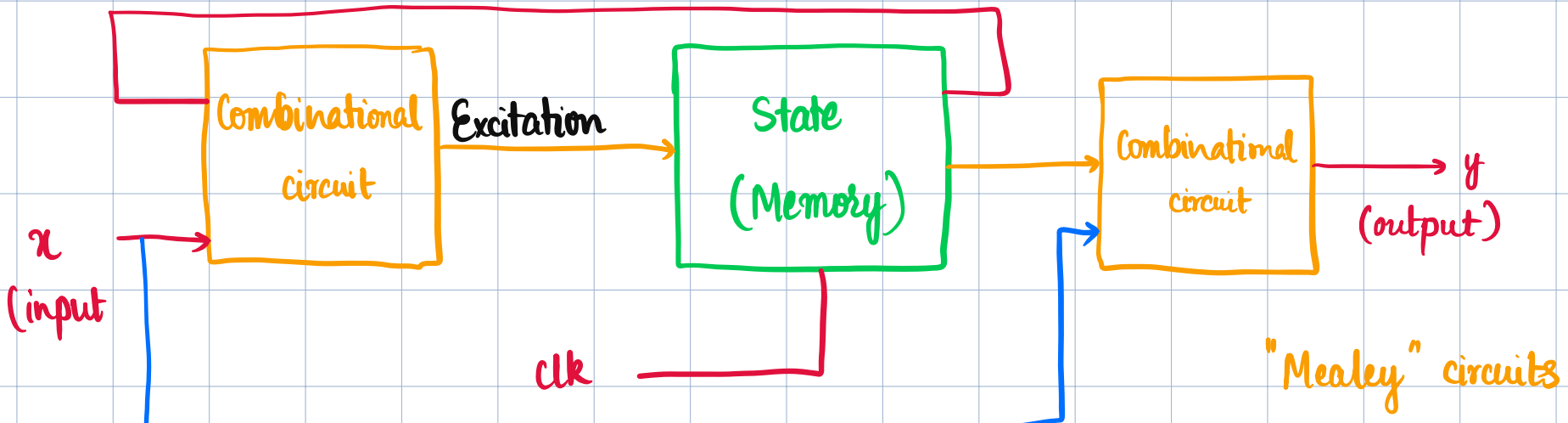
State assignment

	Q_1	Q_2	Q_3
S	0	0	0
A	0	0	1
B	0	1	0
C	0	1	1
D	1	0	0

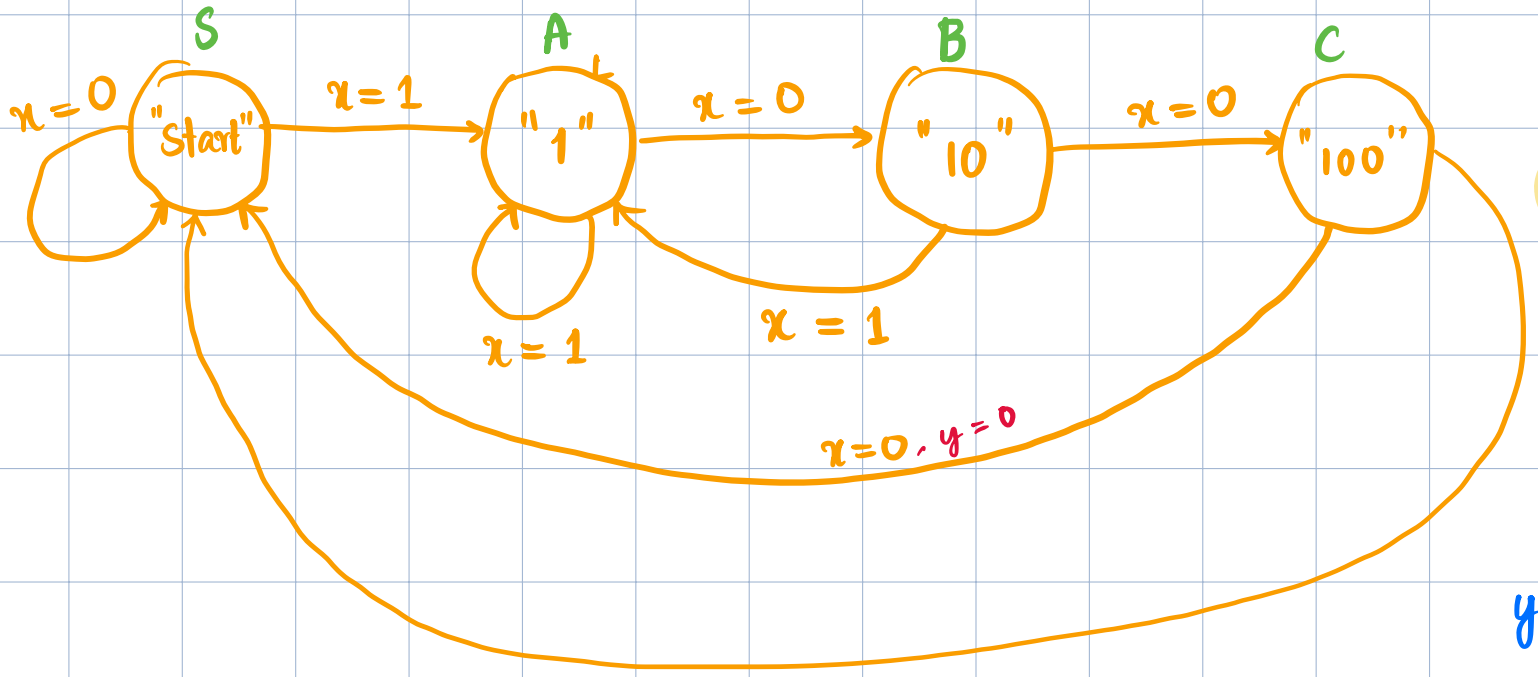
x	Present state	Next state	J_1 K_1	J_2 K_2	J_3 K_3
0	0 0 0	0 0 0	0 x	0 x	0 x
1	0 0 0	0 0 1	0 x	0 x	1 x
0	0 0 1	0 1 0	0 x	1 x	x 1
1	0 0 1	0 0 1	0 x	0 x	x 0




Combinational circuit
Excitation
State (Memory)
Combinational circuit
x (input
clk
y (output)
Output is derived from the state [FF o/p]
"Moore" circuits


Combinational circuit
Excitation
State (Memory)
Combinational circuit
x (input
clk
y (output)
"Mealey" circuits

Moore circuit to Mealey circuit



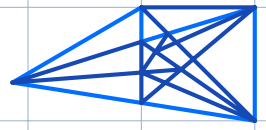
x = 1 , y = 1

↓

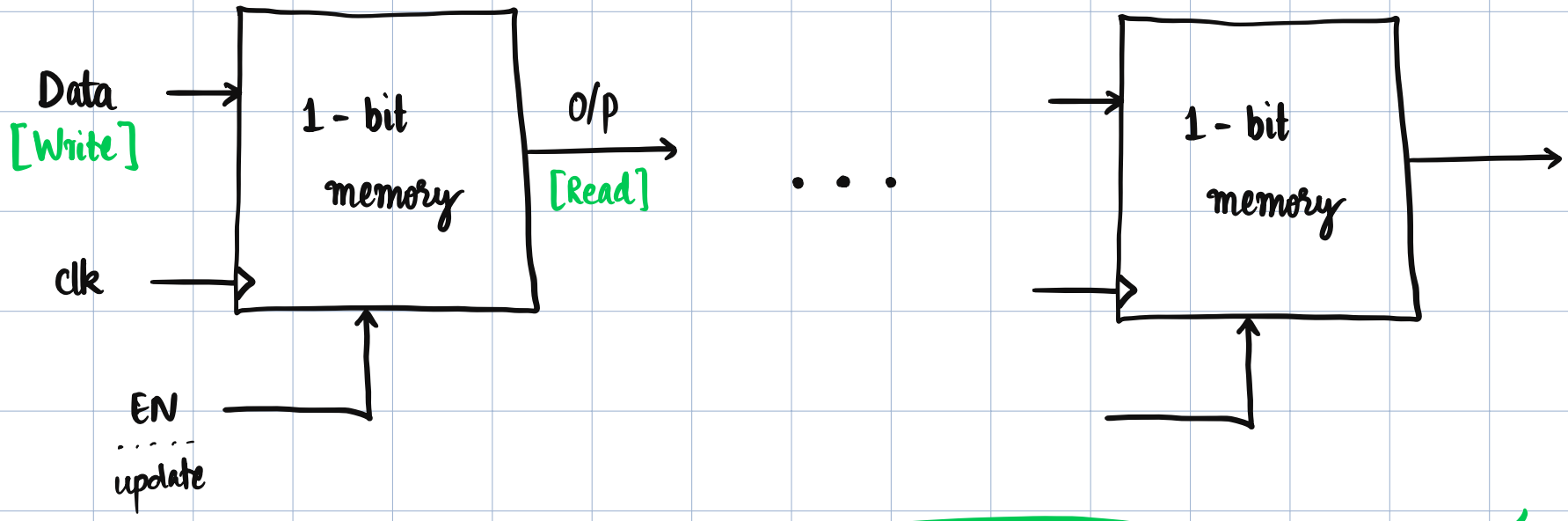
y depends on x directly

↓

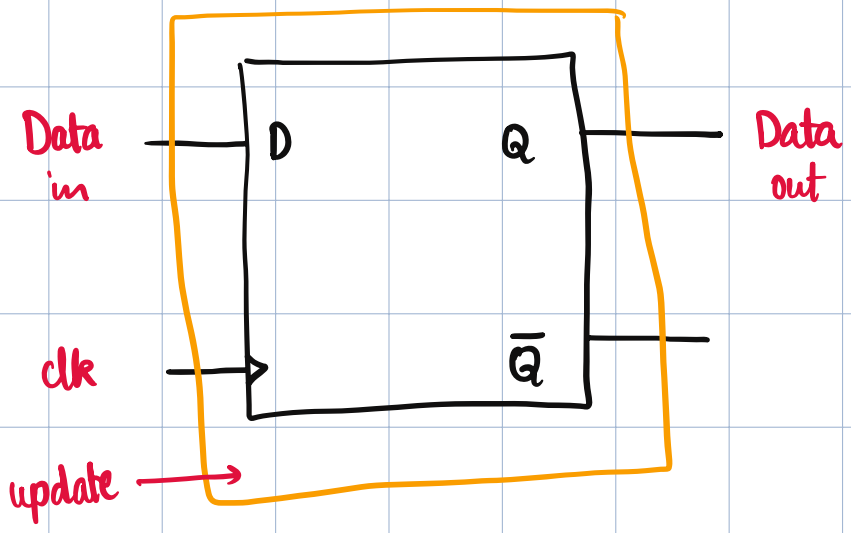
y may not be synchronized with the clock if x is non-synchronous

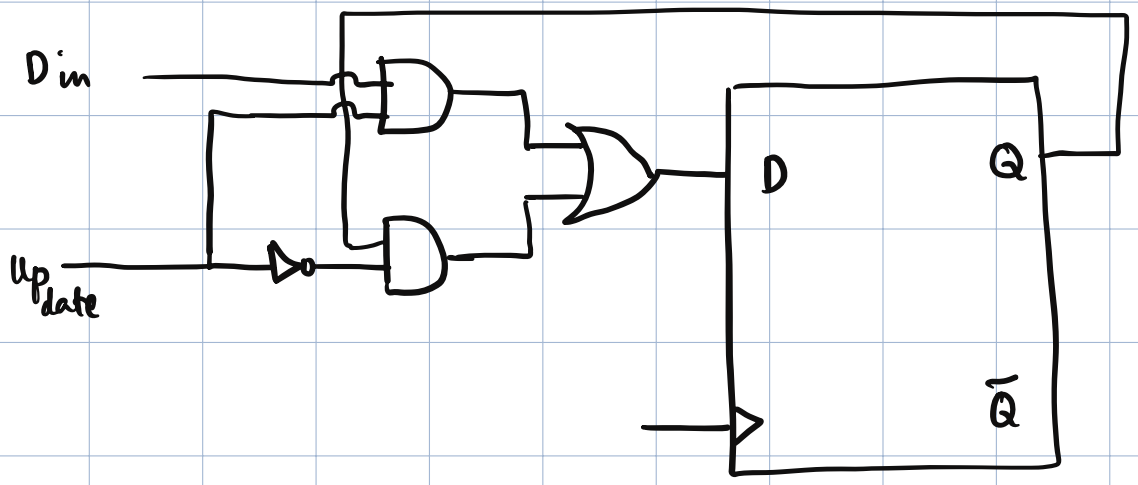


8 bit ⟶ 1 byte

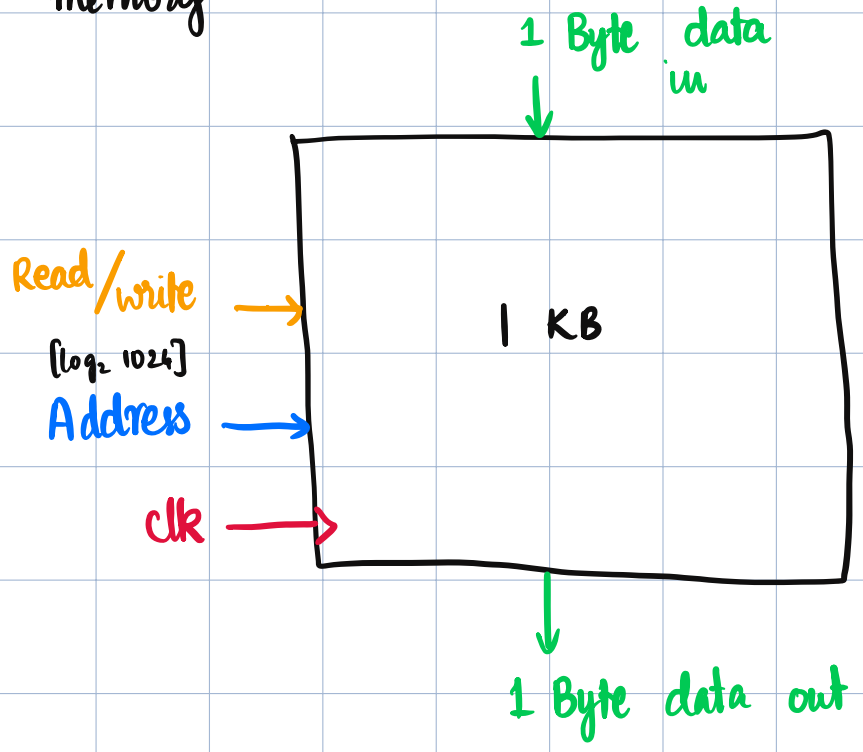


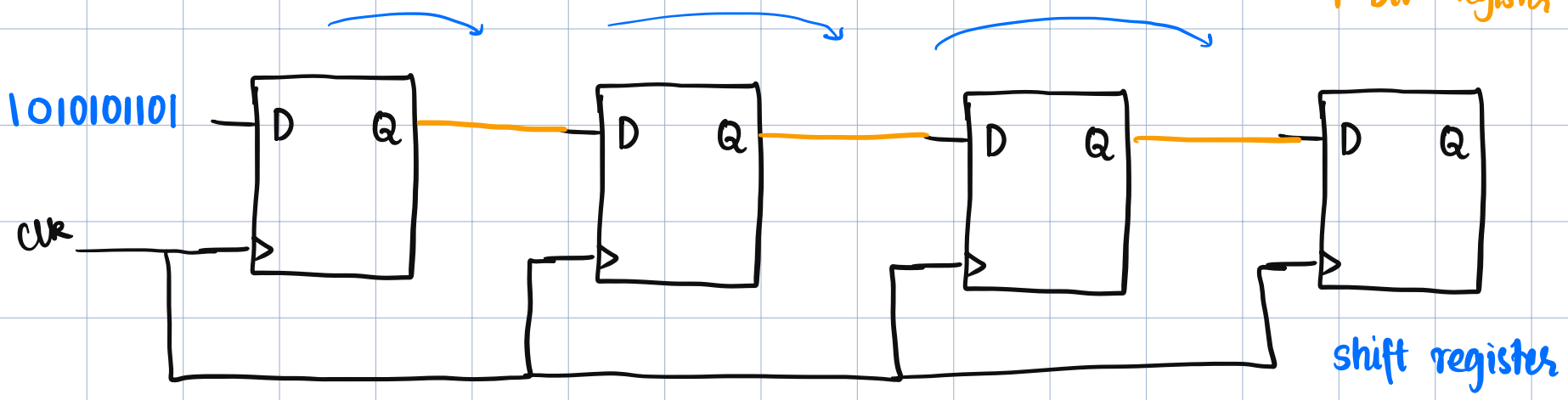
8 single - bit memory element


Data in
D
Q
Data out
clk
$\bar{Q}$
update


D in
Update
D
Q
$\bar{Q}$

1 KB memory


1 Byte data in
Read/write
[log2 1024]
Address
clk
1 KB
1 Byte data out


4 bit register
1010101101
clk
D
Q
shift register