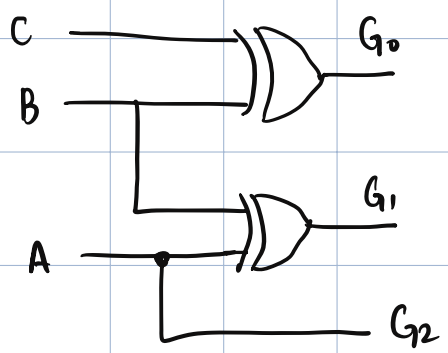
10 Nov 2024 – Digital Circuits

Gray code

$G_0 = B \oplus C$

$G_1 = A \oplus B$

$G_2 = A$



A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

G_2	G_1	G_0
0	0	0
0	0	1
0	1	1
0	1	0
1	1	0
1	1	1
1	0	1
1	0	0

$(46)_8$ —gray code→

$6 + 8 \times 4 = (38)_{10}$

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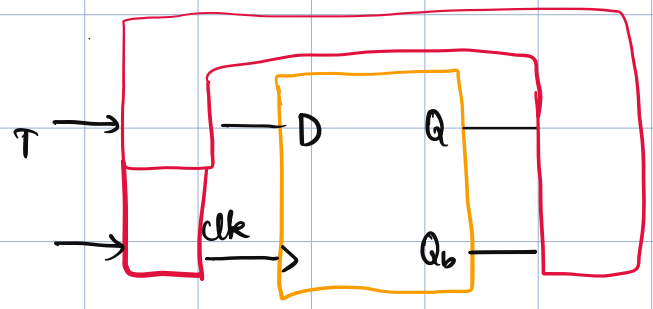
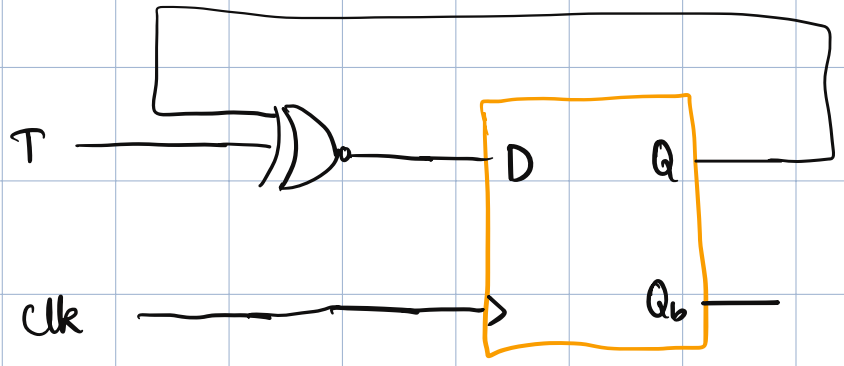
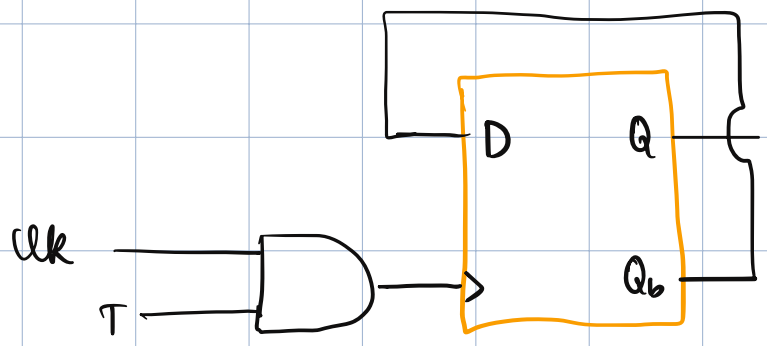
11 Nov 2024 - Digital Circuits - Week 15



Clk	T	Q
↓	x	Q^*
↑	0	Q^*
↑	1	$\overline{Q^*}$



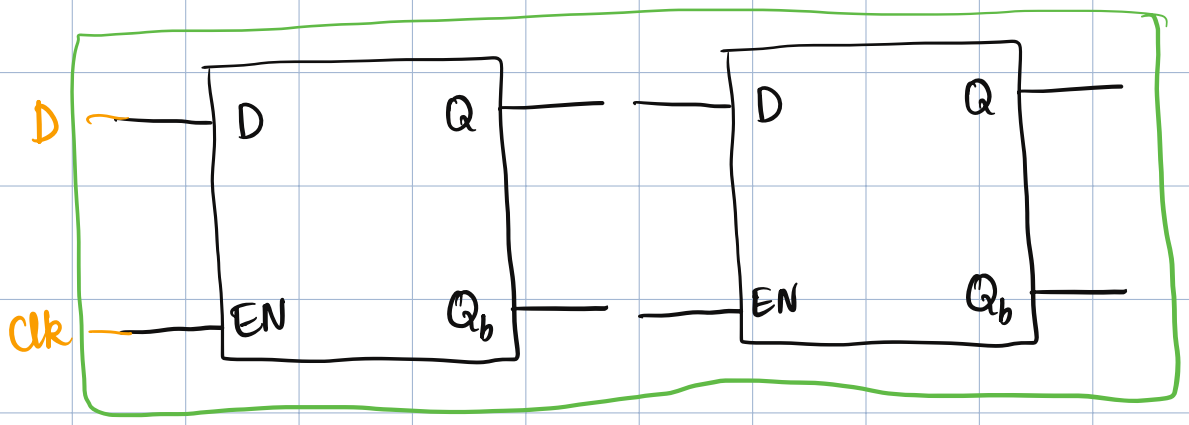
T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0



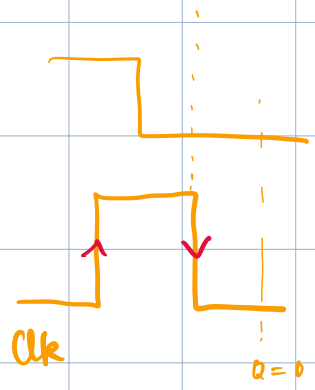
"T Flip-flop"

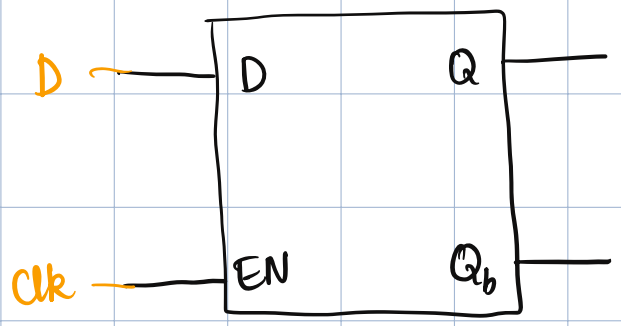
→ simple toggling behaviour

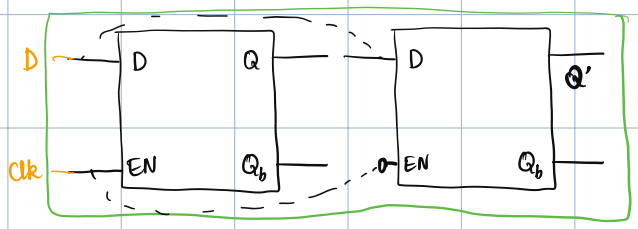
→ can be used in counting

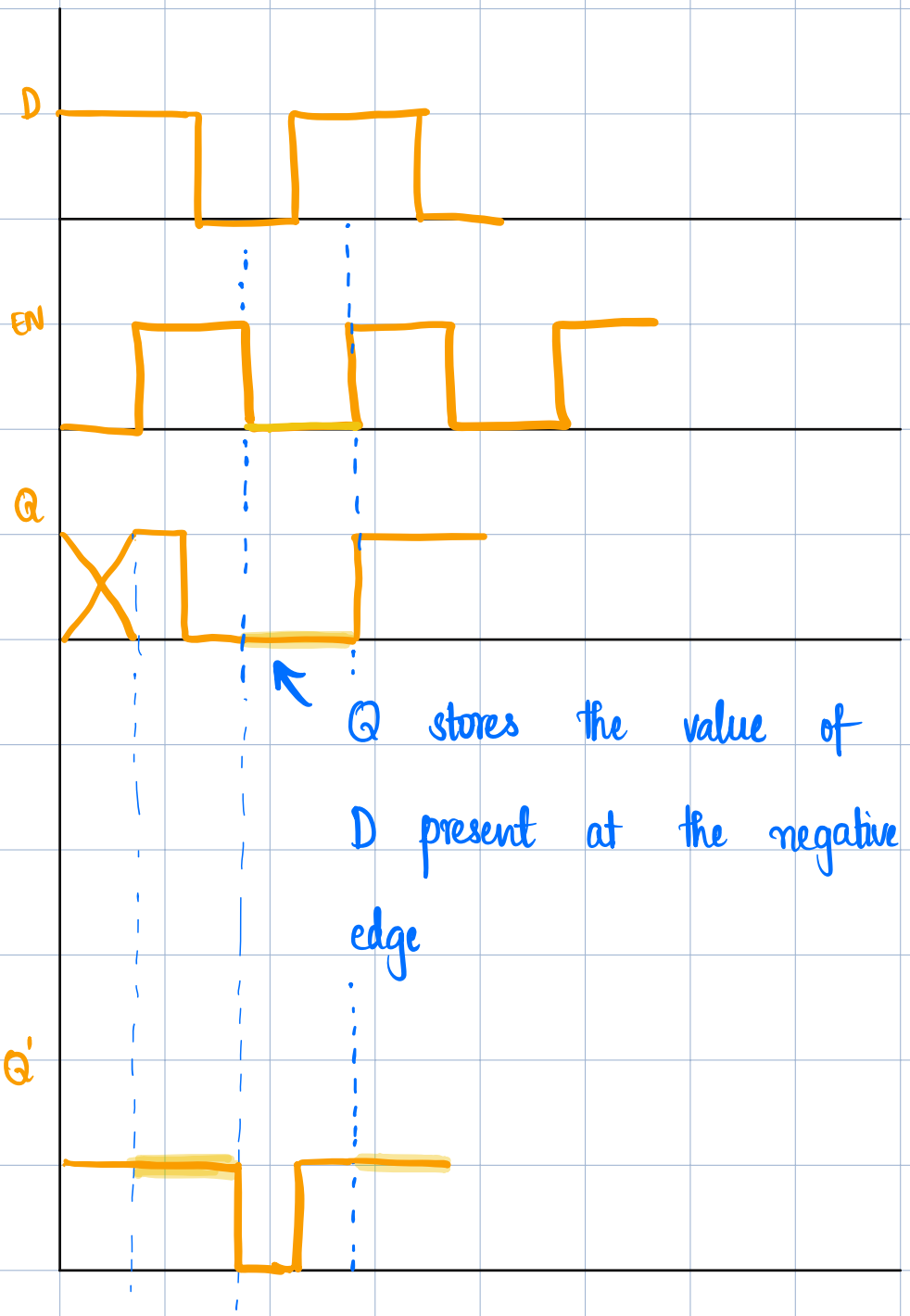


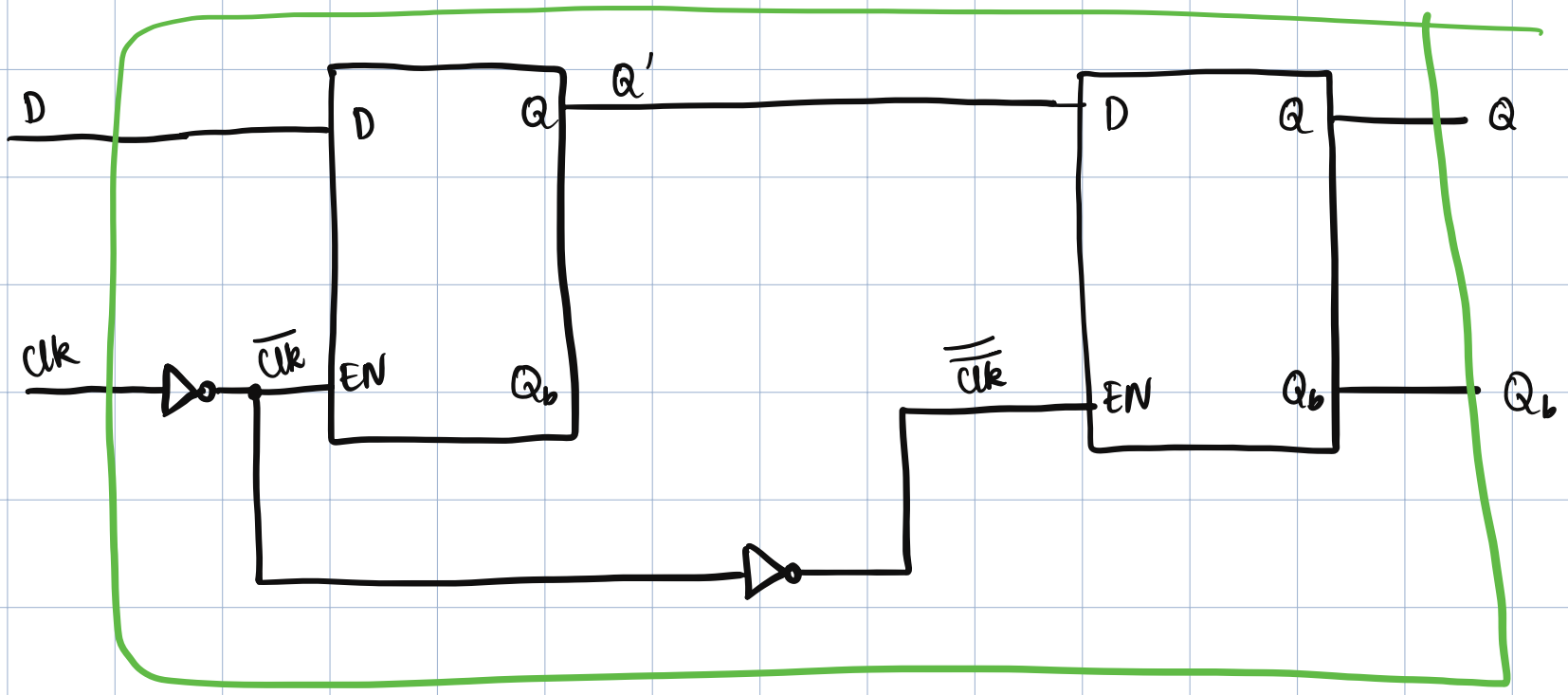
Add an edge sensitivity with more than 1 latch

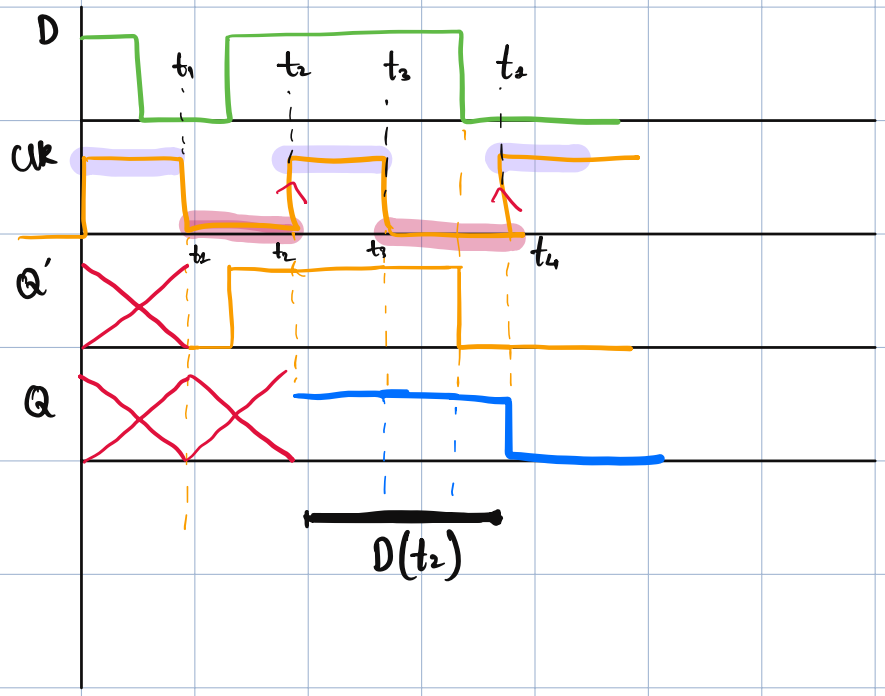



D
Clk
D
Q
EN
Q_b


D
Clk
D
Q
EN
Q_b
D
Q'
EN
Q_b


D
EN
Q
Q stores the value of D present at the negative edge
Q'

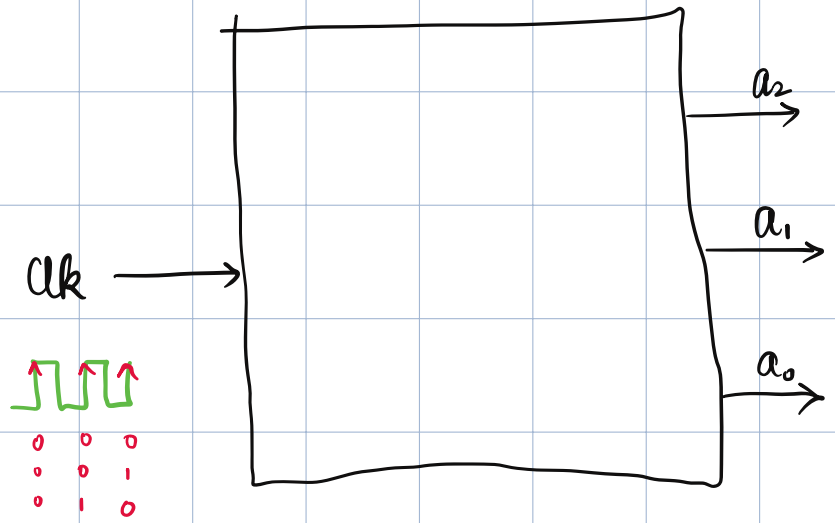




Master - slave

D flip-flop

13 Nov 2024



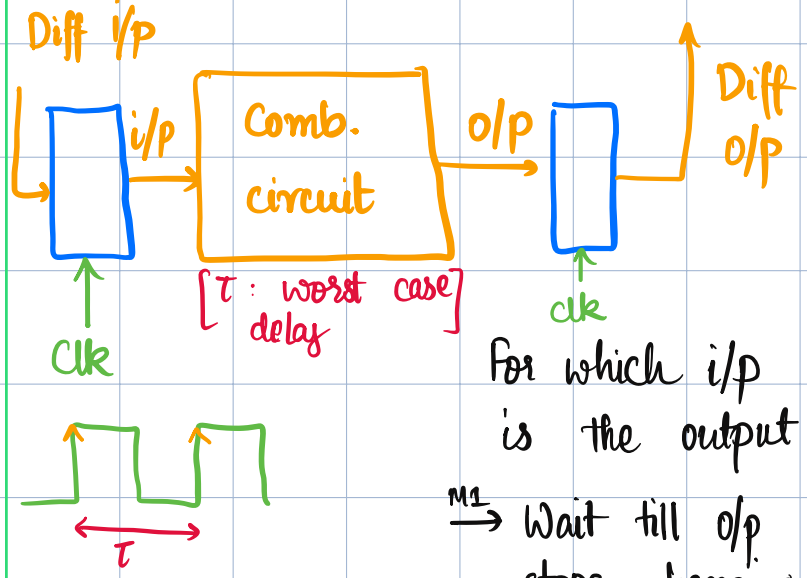
Clk	a_2	a_1	a_0
↑	0	0	0
↓	0	0	1
↑	0	1	0
↓	0	1	1

temp., etc.

3 inverters in a loop racing

LC circuits

Clk signal → periodic



For which i/p is the output?

M1 → Wait till o/p stops changing

to automate this, we add clock signal

M2 → Wait for worst case delay

1 MHz

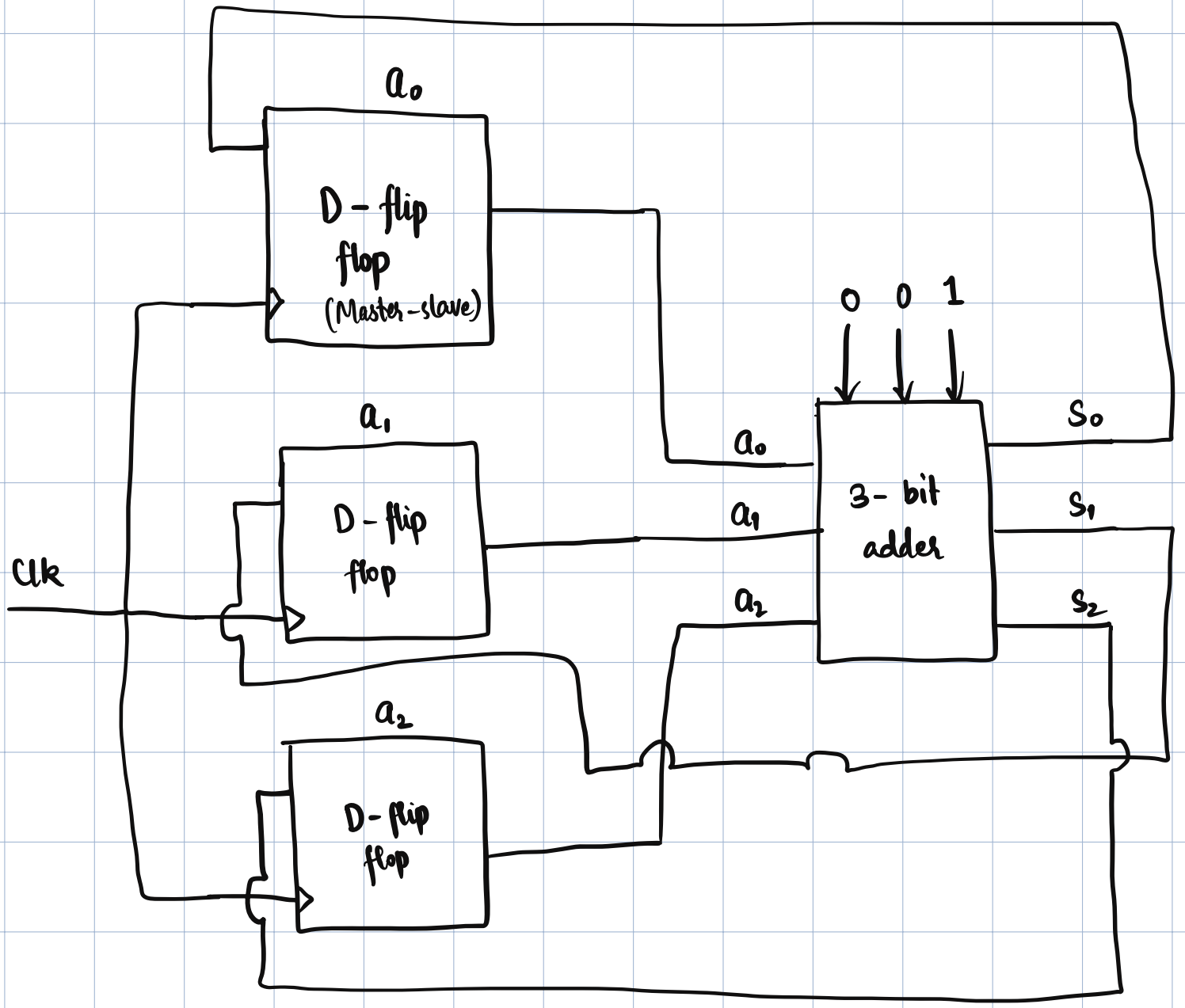
ref clk out side

more clks

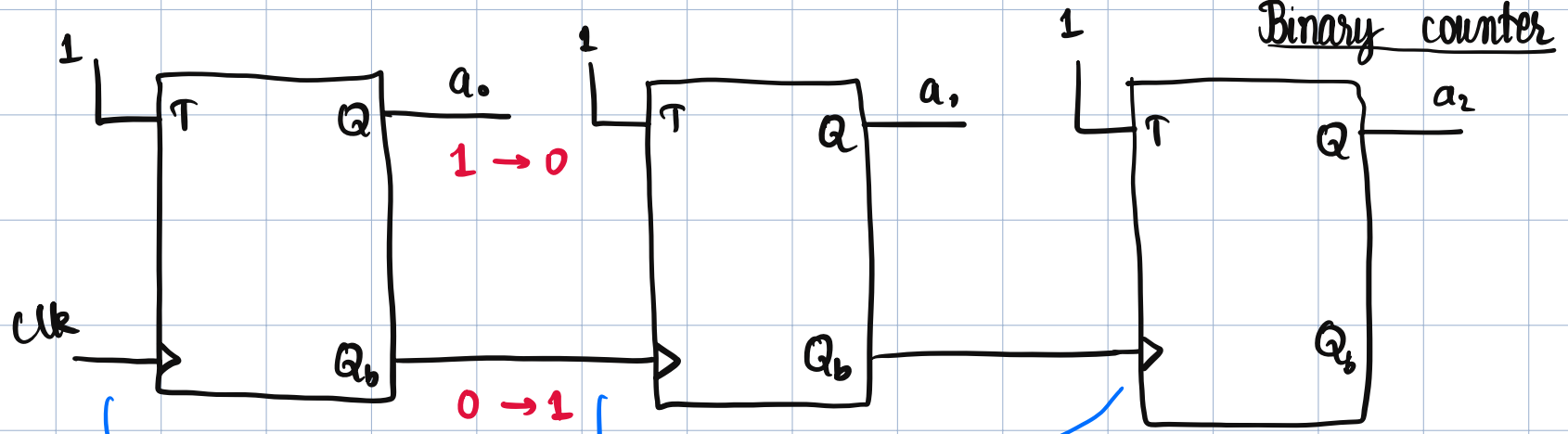
IC

use a piezoelectric material

mechanical force → electric field


a_0
D - flip flop (Master-slave)
a_1
D - flip flop
a_2
D - flip flop
Clk
0 0 1
a_0
a_1
a_2
3 - bit adder
S_0
S_1
S_2

Binary counter



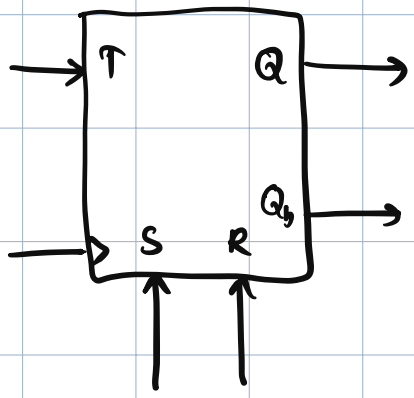
ripple effect

Different flip-flops have different clock signals

⇓

Their o/p will not change together

Asynchronous sequential circuit



Set Reset

Forces the flip-flop to start in a known state