2024/11/03 - Digital Circuits - Week 14

Tutorial 5 discussion

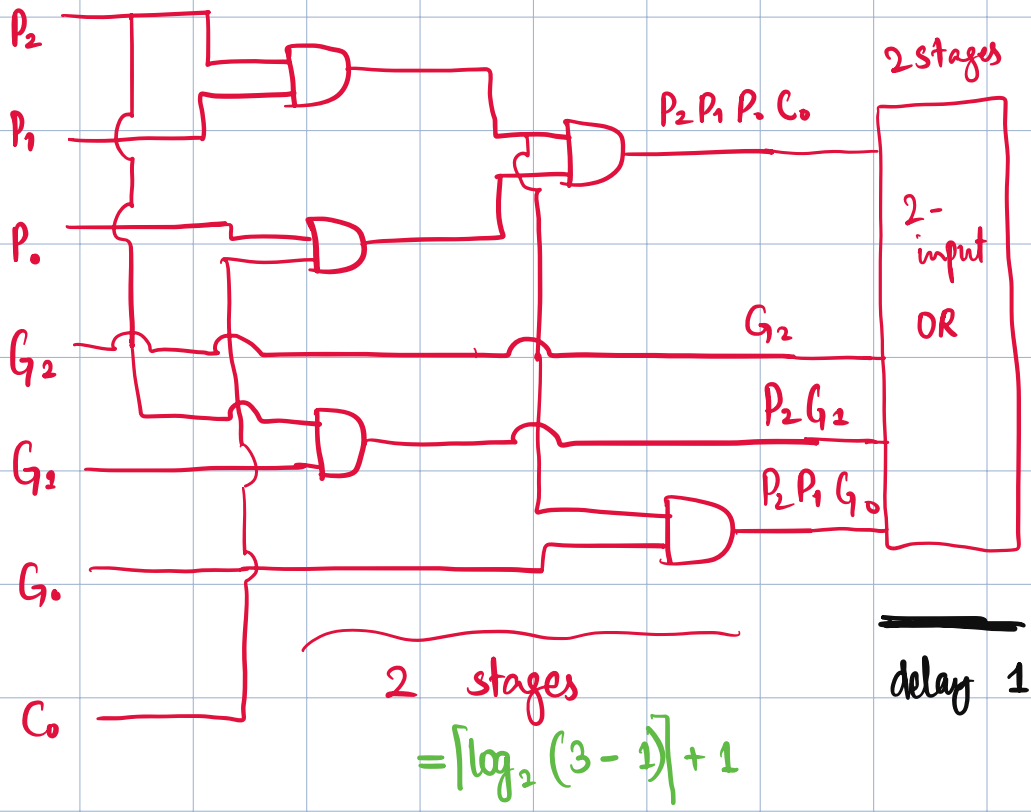
$$C_3 = f(a_2, b_2, C_2)$$

$$= P_2 \cdot C_2 + G_2$$

$$= P_2 \left[P_1 \cdot (P_0 C_0 + G_0) + G_2 \right] + G_2$$

$$= P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$$

e.g.: 3-bit adder



n-input gates are available

⇓

1 (XOR and) + 2 (SOP) = 3 unit delays

2-input gates

1 (XOR AND) +

for n - bit input (assume n is even)

delay is determined by delay in computation of

$$P_{n-1}\ P_{n-2}\ \cdots\ P_1\ P_0\ C_0$$

and the delay of OR

6. ~

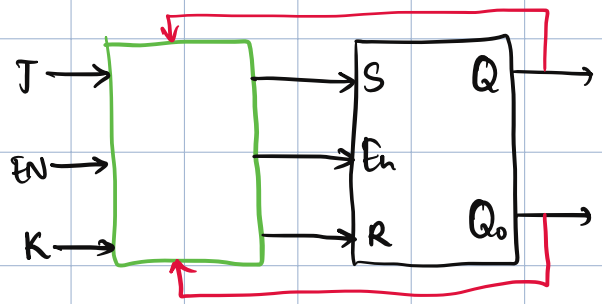
* verify

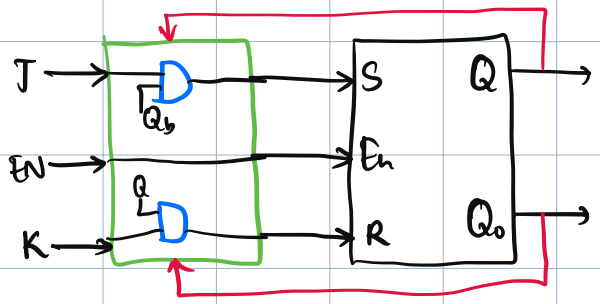
$$C_4 = P_3 G_2 + G_3$$

$$=$$

06 Nov 2024

"J-K latch"



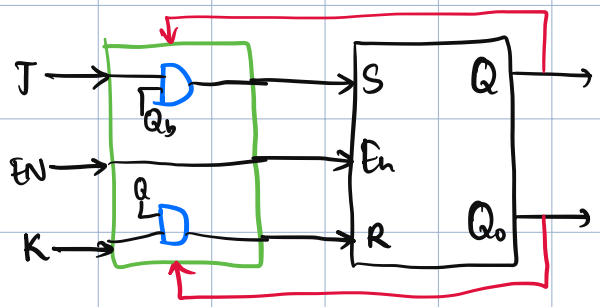


EN	J	K	Q	Q_b	
0	x	x	Q^*	Q_b^*	→ store
1	1	0	1	0	→ set
1	0	1	0	1	→ reset
1	0	0	Q^*	Q_b^*	→ store
1	1	1	$\overline{Q^*}$	$\overline{Q_b^*}$	→ toggle

→ toggling forever (racing condition)

→ How to toggle only once?

→ stop toggling after a delay.



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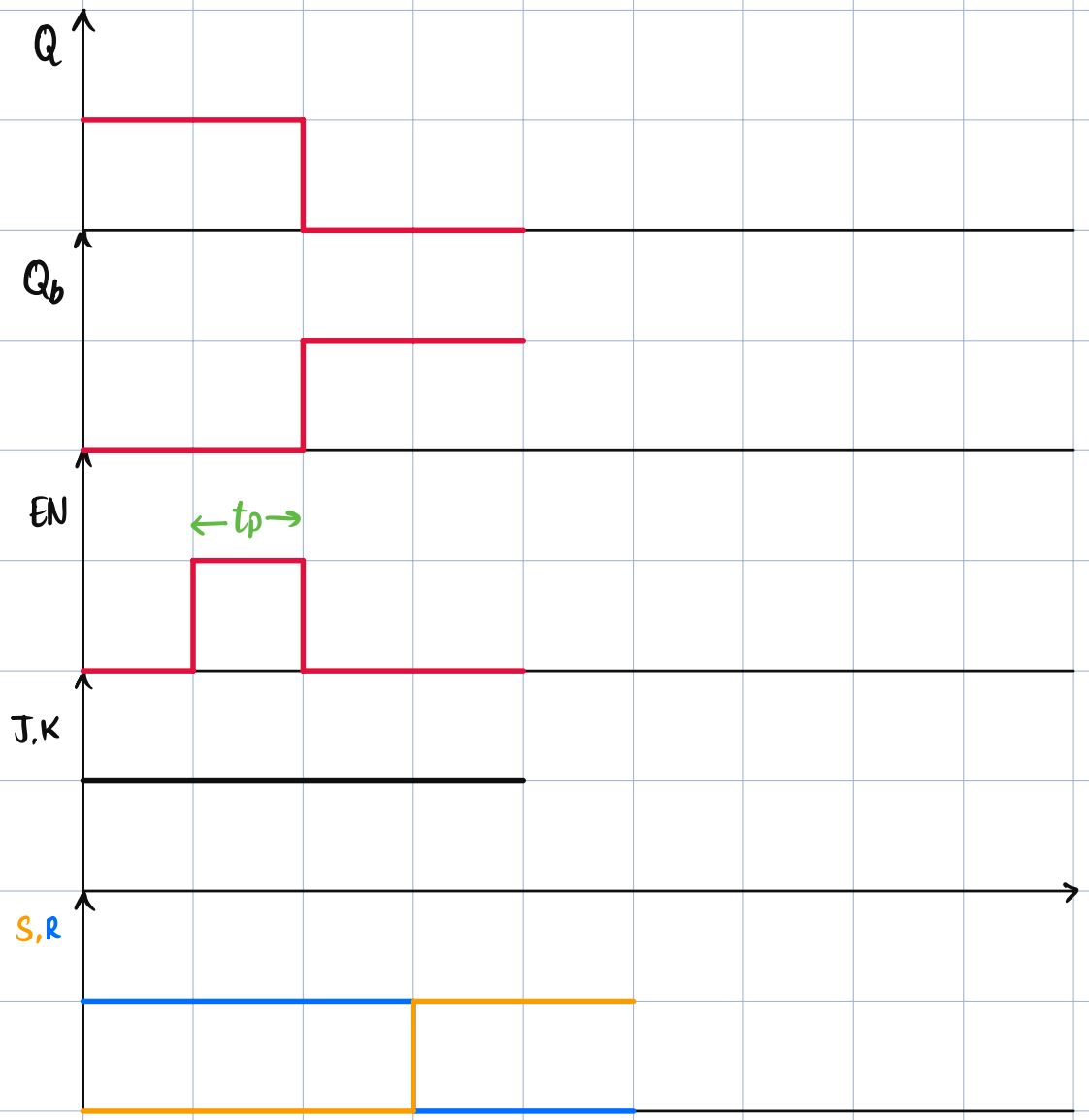


Starting state: $S = 0$, $R = 1$,

$EN = 0$

EN → should be a pulse (to not keep toggling)

length should be ≥ EN → Q delay

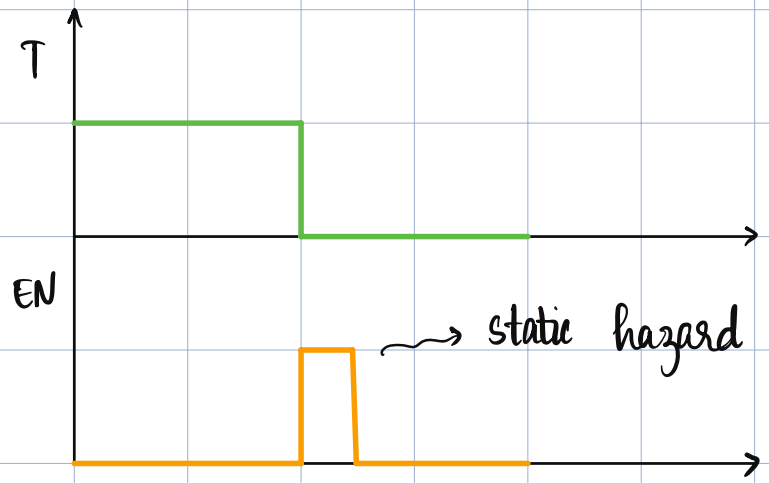
≤ S-R change ⊗

??

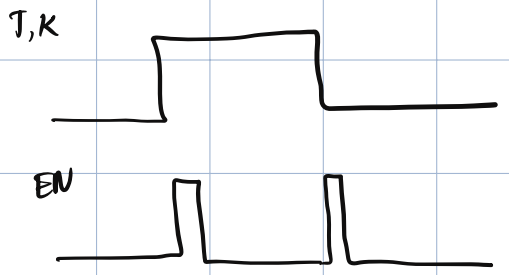
$t_p > t_{min}$ ⇝ metastability

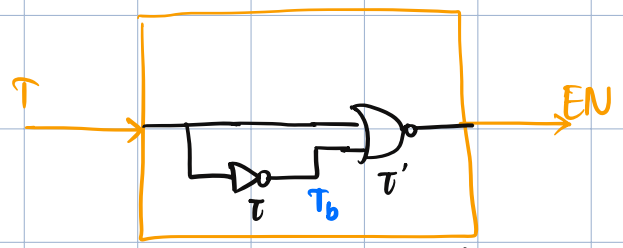
$t_p < t_{EN-Q} + t_{AND}$

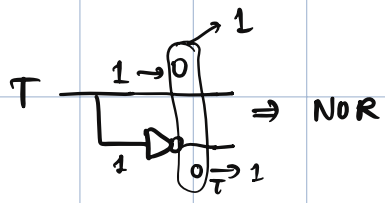
Alternate : EN to AND gates with J and K.



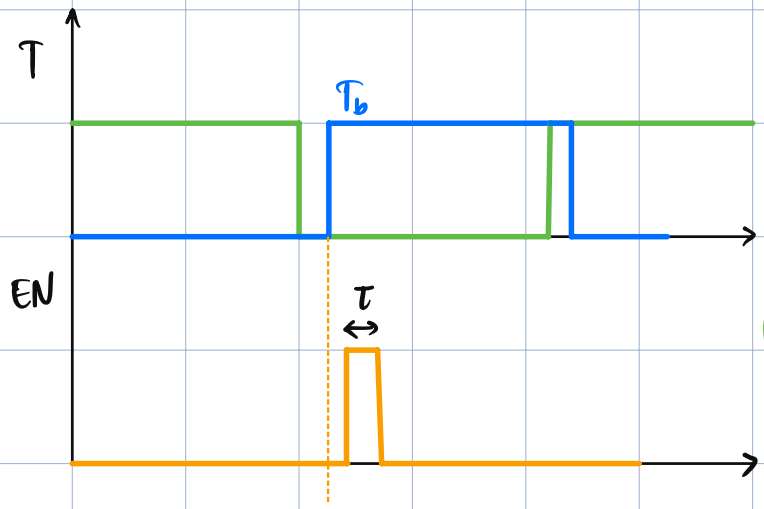
generate a narrow pulse whenever there is a change in J, K



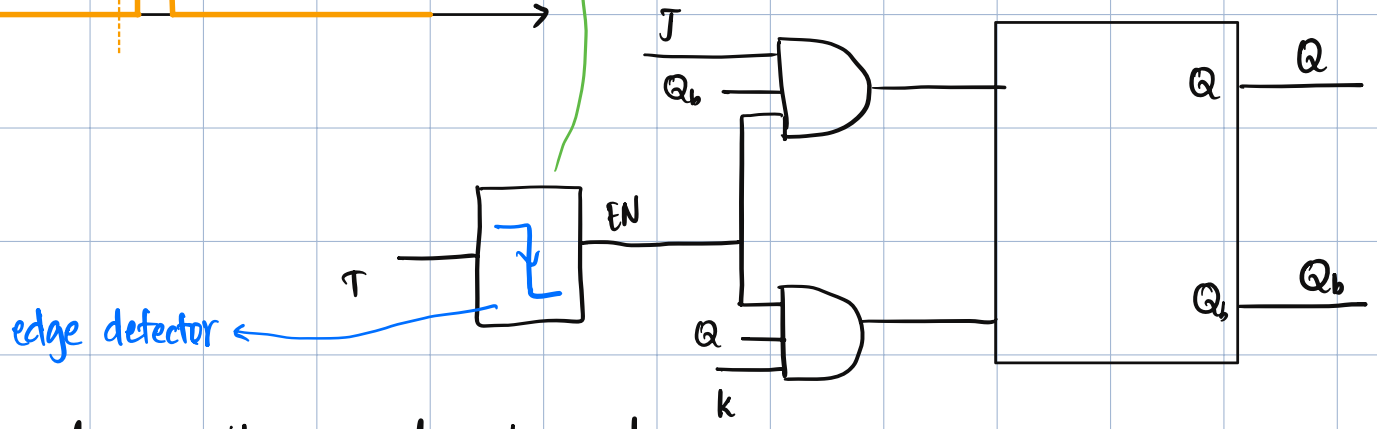




→ Negative edge detector



edge detector circuit has converted a level-triggered latch into edge-triggered flip-flop



level triggered circuit → edge triggered

J and K have meaning only when T changes

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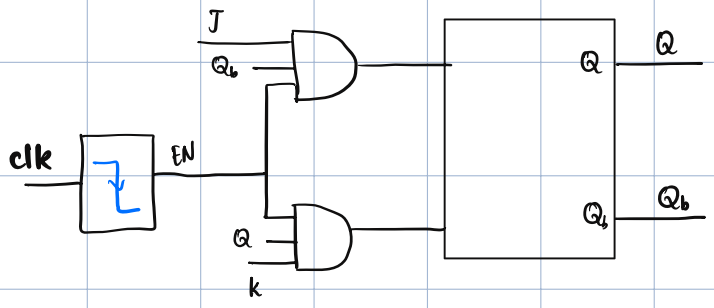
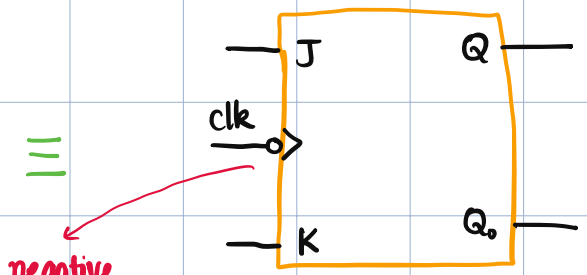
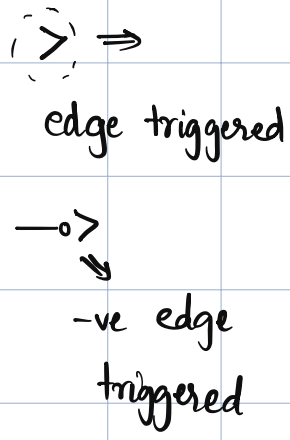
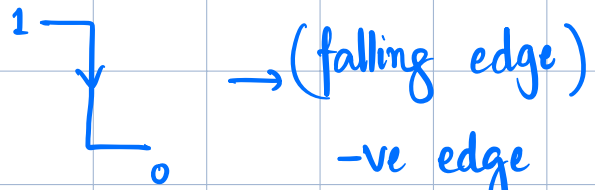




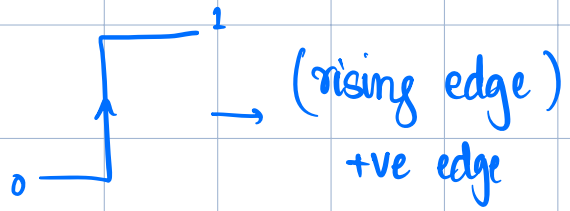
negative edge-triggered





→ (falling edge)

-ve edge



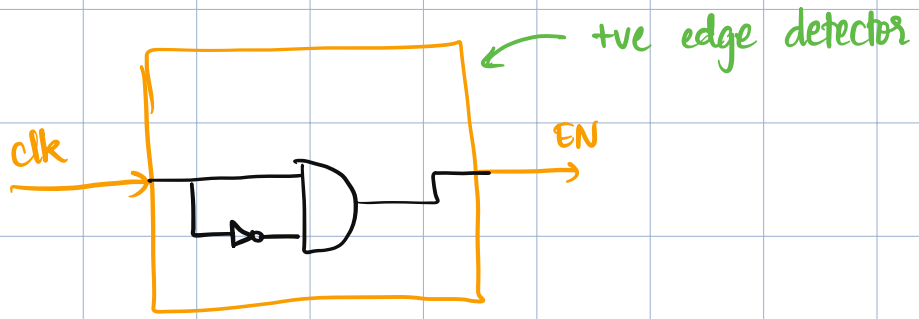
→ (rising edge)

+ve edge

Clk	J	K	Q
0	x	x	Q^*
1	x	x	Q^*
↑	x	x	Q^*
↓	0	0	Q^*
↓	0	1	0
↓	1	0	1
↓	1	1	$\overline{Q^*}$

+ve edge →

-ve edge →



Is it more desirable to have +ve edge triggered flip-flop?

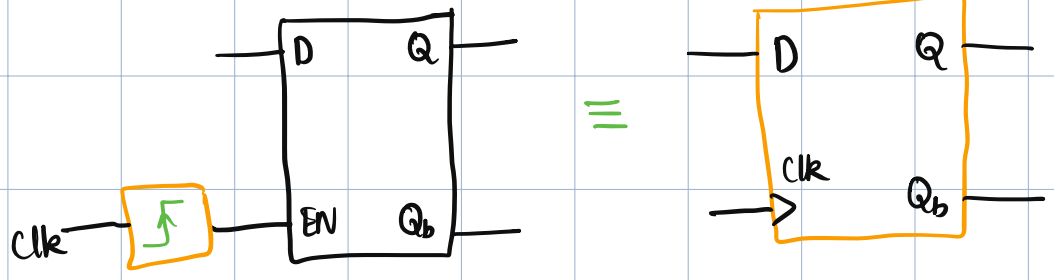
pmos nMOS

↓

one of them is better depending on the technology

→ better one has sharp edge (less uncertainity

D- latch



cascade

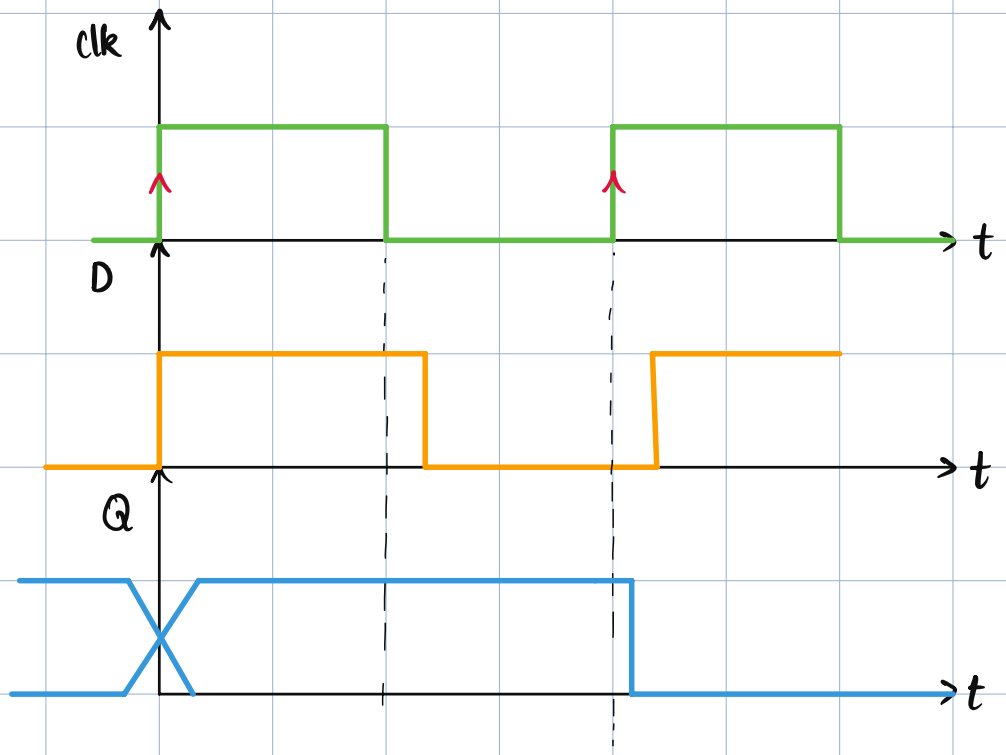
+ve edge triggered and -ve edge triggered latches

↓

DDR

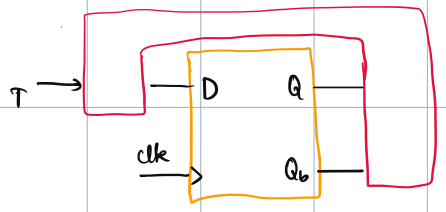
CMOS → easy to discharge

→ NMOS faster than PMOS for same size (same speed ⇒ NMOS ×3 bigger)

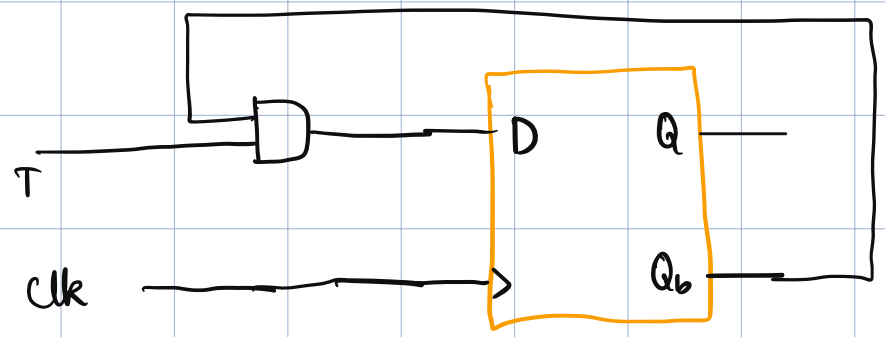


period of clock
↓
based on worst case delay in D ← output of combinational circuit.

toggle ?



clk	T	Q
↓	x	Q^*
↑	0	Q^*
↑	1	$\overline{Q^*}$


T
Clk
D
Q
Q'