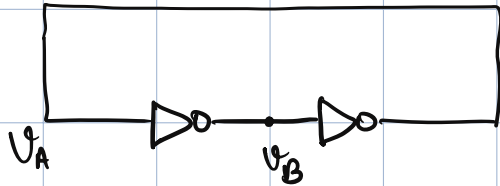
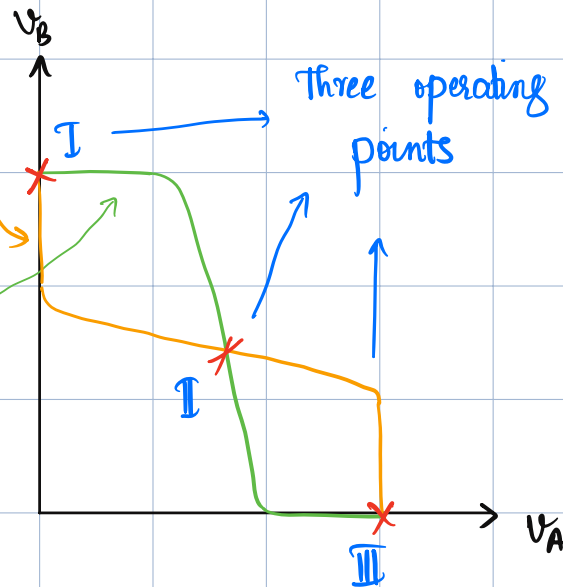
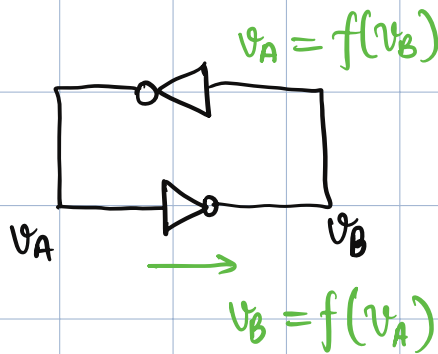


# 2024/10/21 - Digital Circuits - Week 12



III



latch

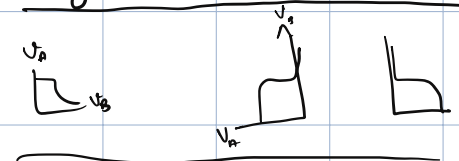
"Bistable"

$V_A$	$V_B$
0	1
1	0

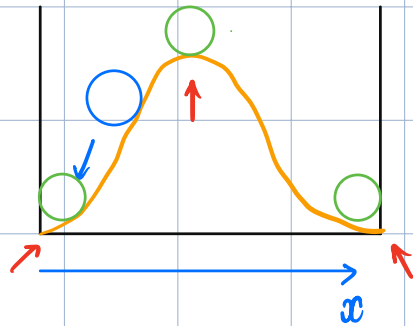
forces  $V_A$  to become 0 again  
 $V_A \rightarrow 0 \rightarrow 0.1 \Rightarrow V_B = 0$  still  
 $V_A \rightarrow \frac{V_{DD}}{2} \uparrow \rightarrow V_B \rightarrow \frac{V_{DD}}{2} \downarrow$   
 $\uparrow \quad \quad \quad \text{II} \rightarrow \text{III}$

Quality of solutions:  
 How good are the operating points?

electrical interference may cause  $V_A$  or  $V_B$  to drift



At these three points signals will remain consistent  
 ( $V_B$  will not force  $V_A$  to change and vice versa)



Three solutions are possible

(I) → unstable operating point

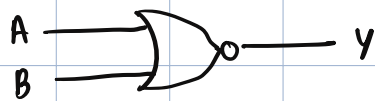
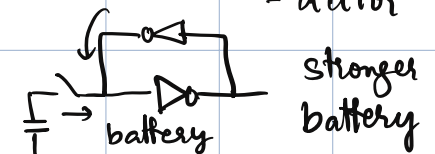
- can be used as storage element.

- how to make the storage useful / dependent on user input?

ideal capacitor

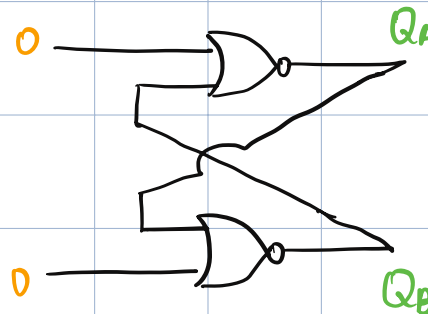
↳ can store ∞ charge

battery ≡ ideal capacitor

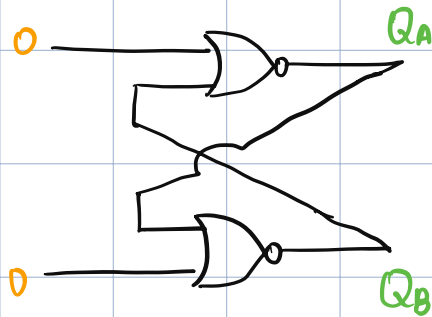


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

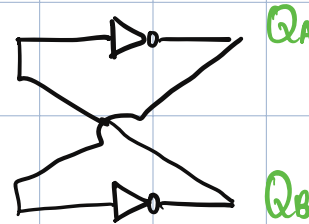
$Y = \bar{B}$



2024/10/23



≡



S	R	QA	QB
0	0	QA*	QB*
0	1	1	0
1	0	0	1
1	1	0	0

last state

set state

reset state

undefined state

→ invalid input (may result in meta-stability)

0 1

$$Q_B = \overline{1 + Q_A}$$

$$= 0$$

$$Q_A = \overline{0 + 0} = 1$$

$$Q_B = \overline{1 + Q_A} = 0$$

$$Q_A = \overline{1 + Q_B} = 0$$

→ NOR gate:

controlled inverter

$$S = 0 = R$$

1 0 } → stays  
or 0 1 } the same  
after applying  
S=R=0

Using first three rows, you can use

the circuit as

a controlled memory

→ state : set of variables in a digital circuit whose value at present instant is sufficient to predict the current O/P based on current input.

→ A digital circuit with  $n$  state variables : finite no. of states.

$Q_A^*$   $Q_B^*$   $\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$  or

$4^{th}$  row  $\rightarrow 1^{st}$  row

$\rightarrow$  unknown state  
 $\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$

$\rightarrow$  Avoid  $4^{th}$  input

$\rightarrow$  Assume output

is not defined

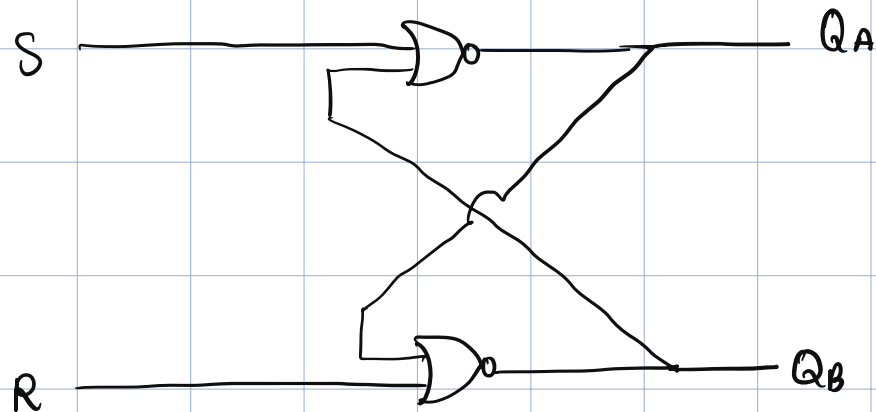
(it is, but

assume)

$\downarrow$

fluctuation after  
changing R & S  
from  $(1, 1)$  to  
 $(0, 1)$  or  $(1, 0)$

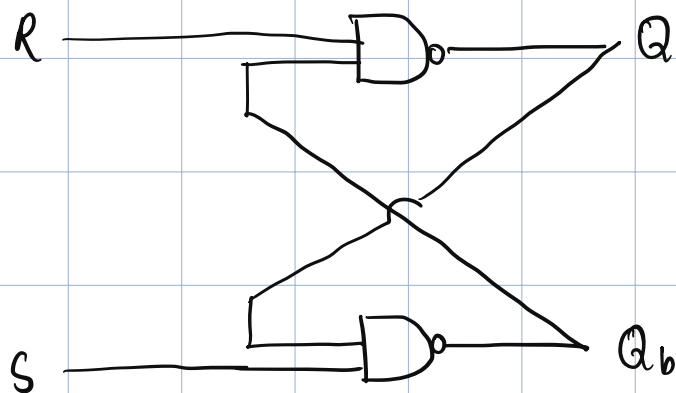
2024/10/24



valid  
inputs  
for  
SR latch

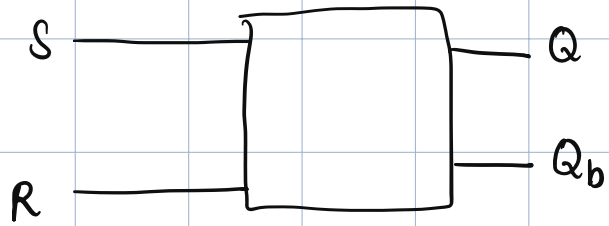
S	R	$Q_A$	$Q_B$
0	0	$Q_A^*$	$Q_B^*$
0	1	0	1
1	0	1	0
1	1	0	0

← Not desired

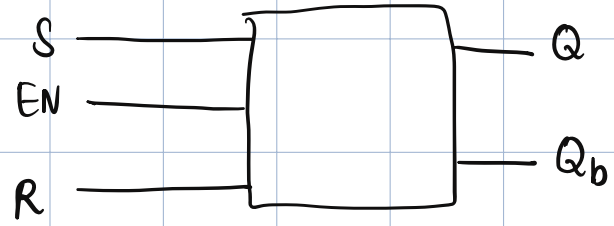


$\bar{S}$ - $\bar{R}$  latch

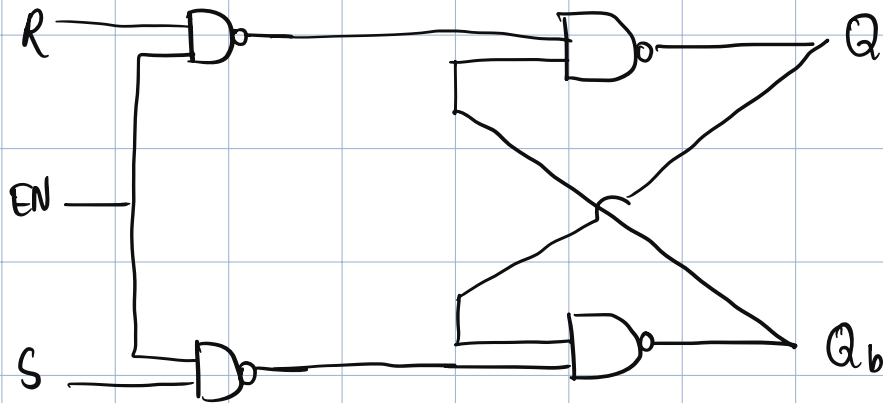
S	R	Q	$Q_B$
0	0	1	1
0	1	0	1
1	0	1	0
1	1	$Q_A^*$	$Q_B^*$



SR latch

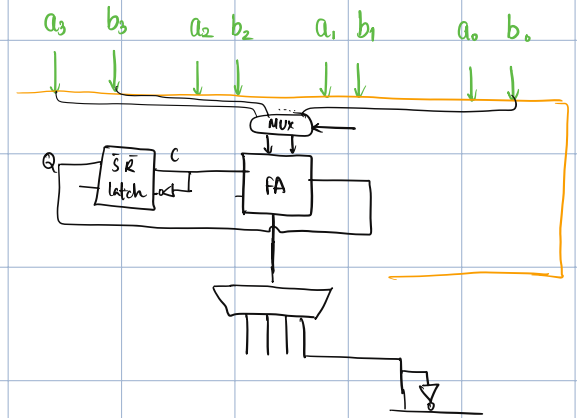
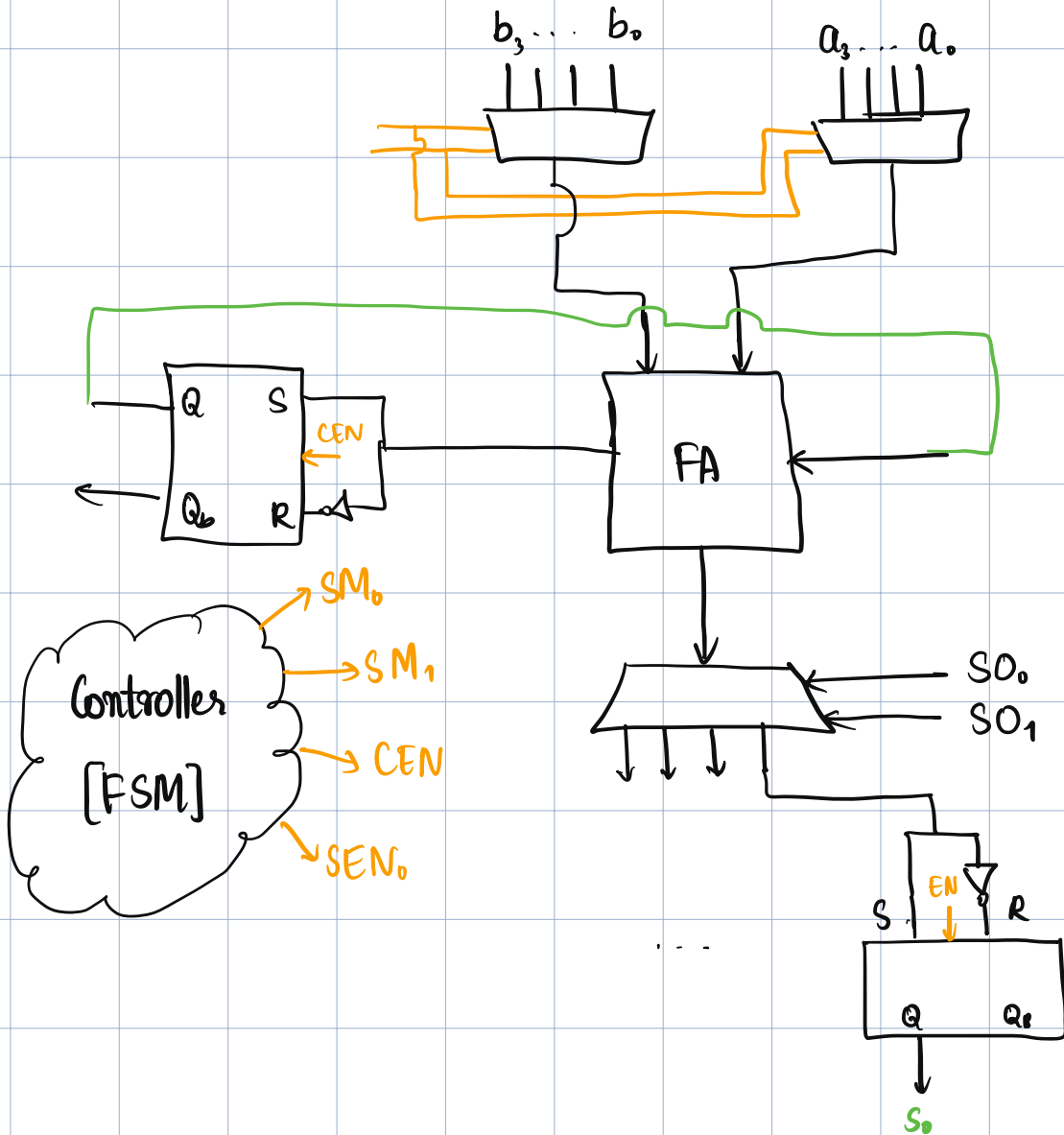


SR latch with enable



→ used in caches

Ex:- 4 bit adder using only one instance of FA and latches, MUX, decoder



← Finite state machine