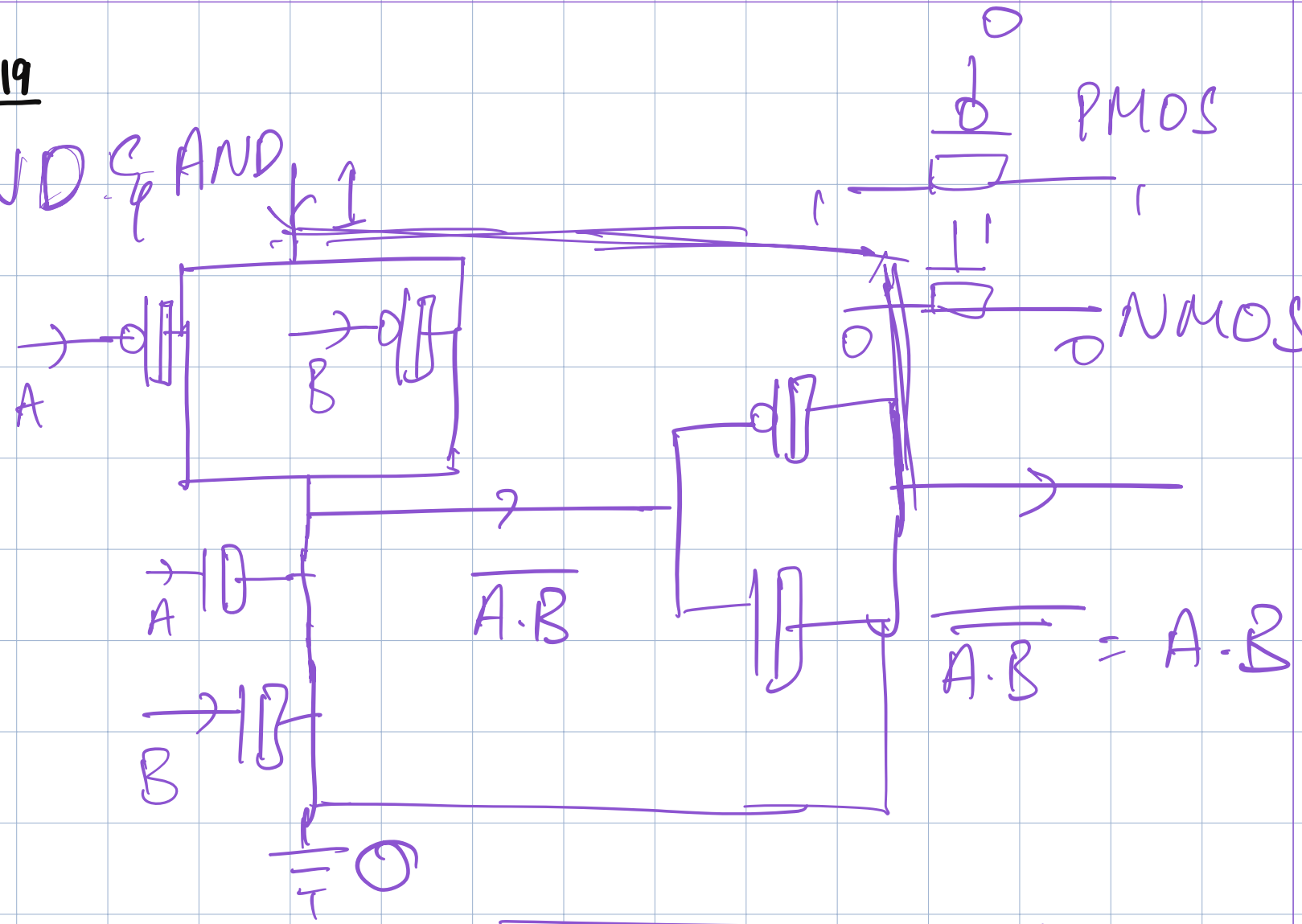
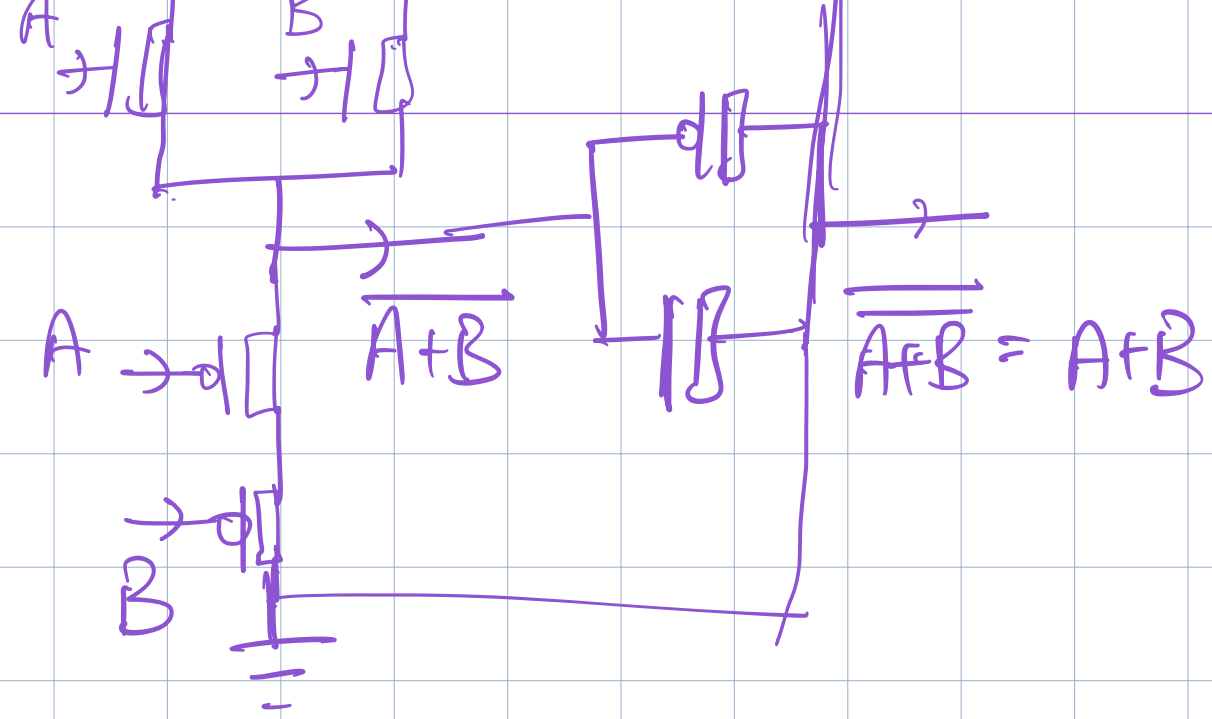
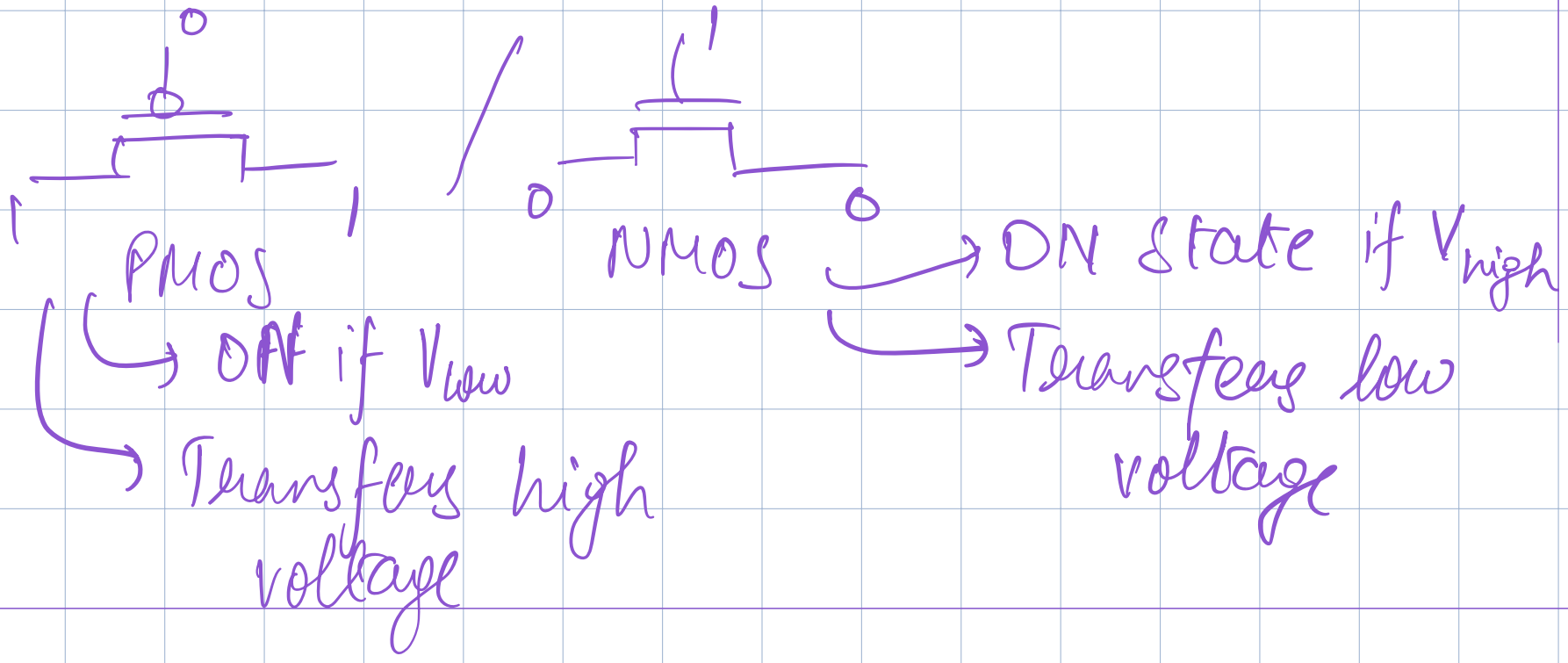
2024/08/19

NAND & AND

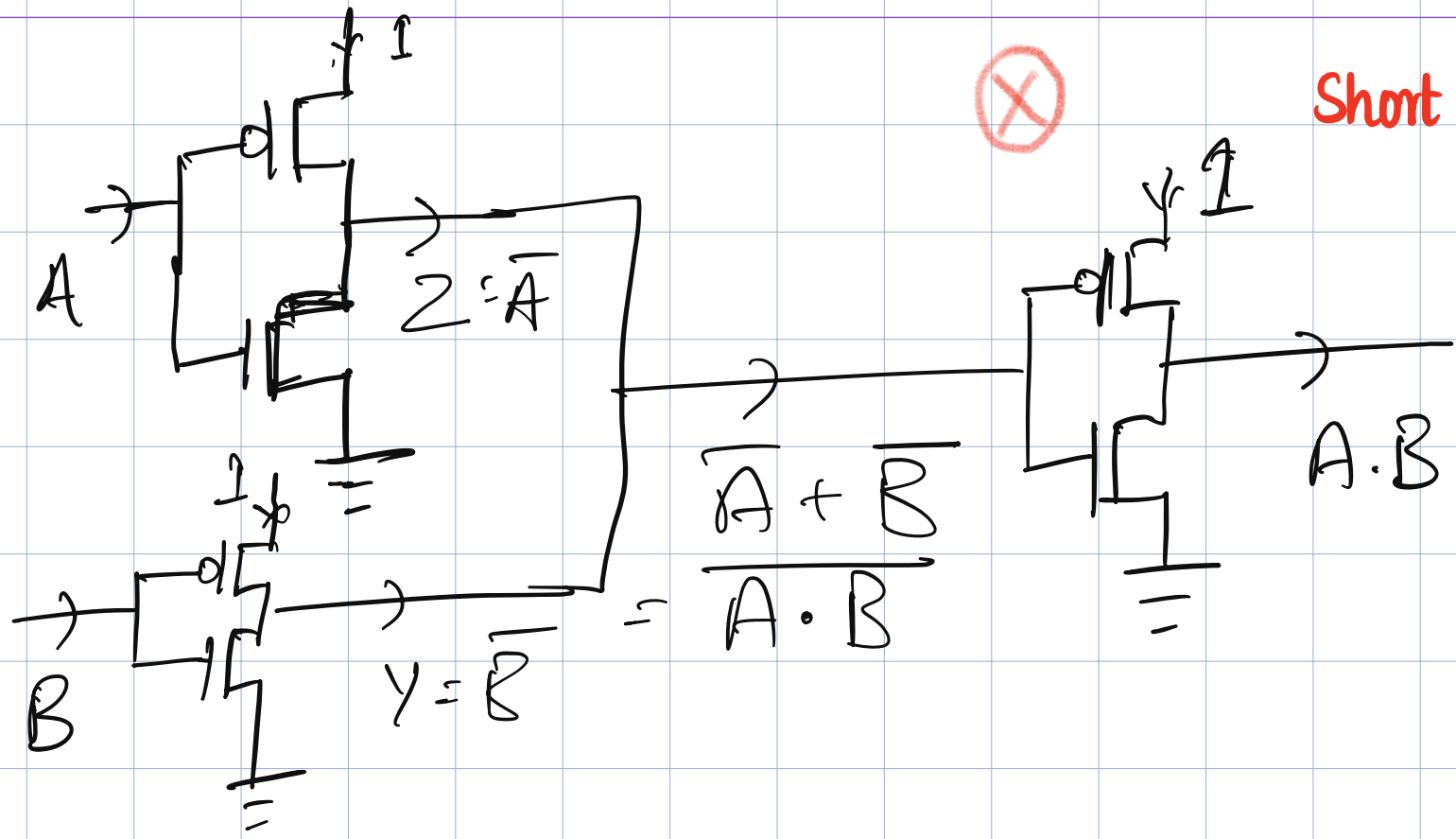


NOR & OR :-

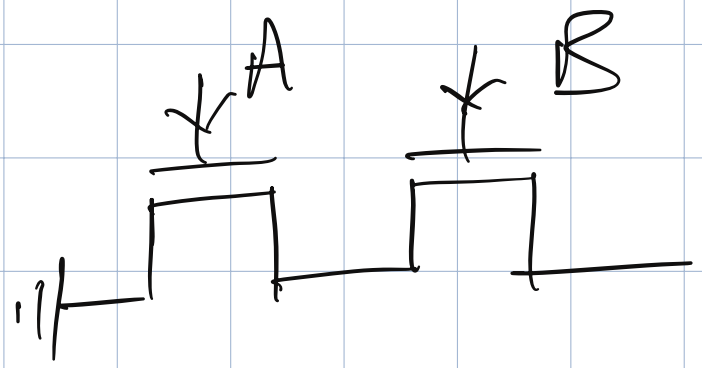

A
B
A
B
A+B
A+B = A+B


0
1
1
PMOS
OFF if V low
Transfers high voltage
1
0
0
NMOS
ON state if V high
Transfers low voltage

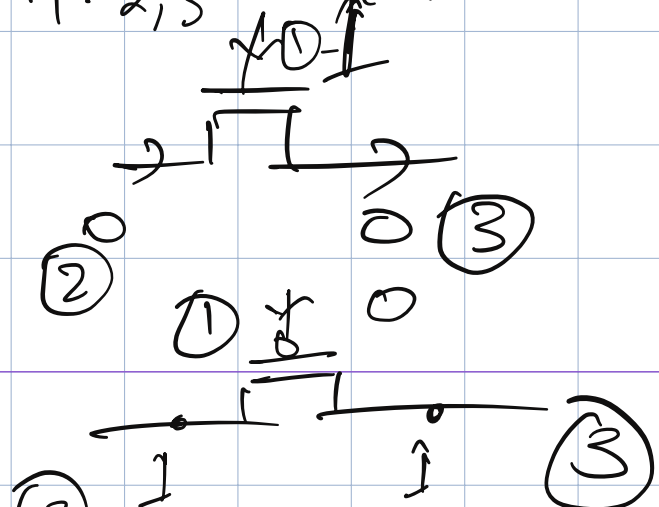
NAND, alternatively:

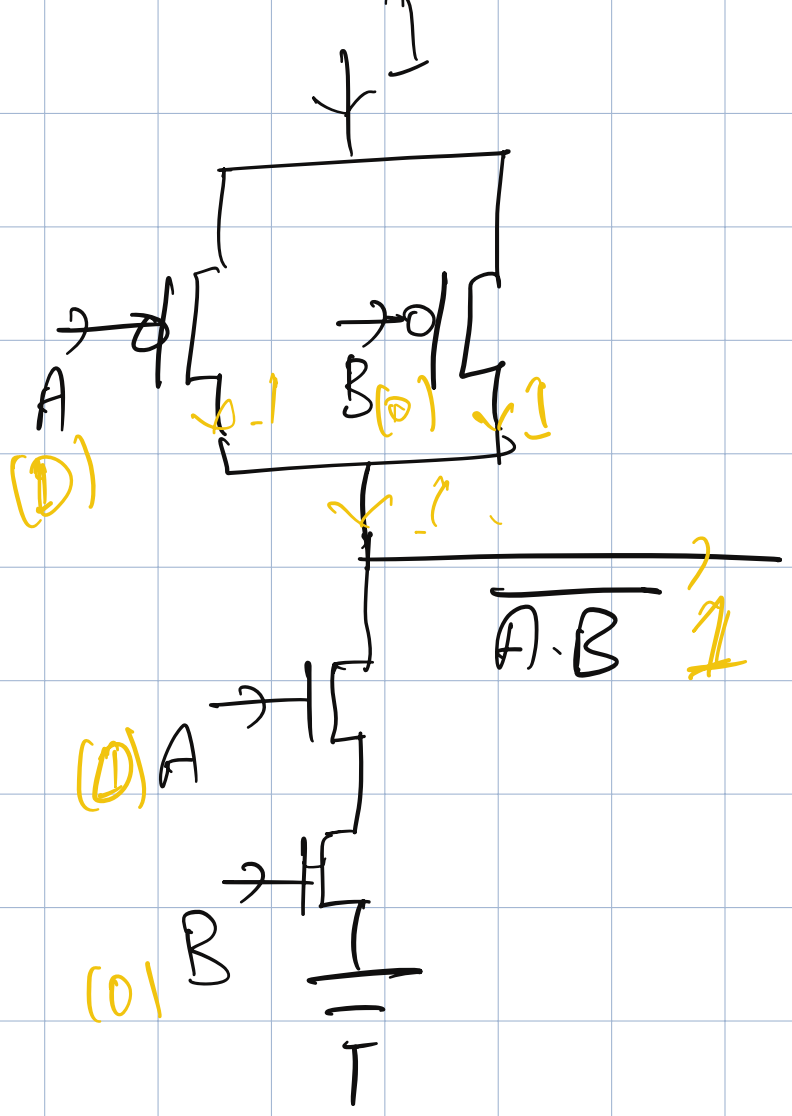


Short circuit



$V_{1-2,3} > V_{th}$

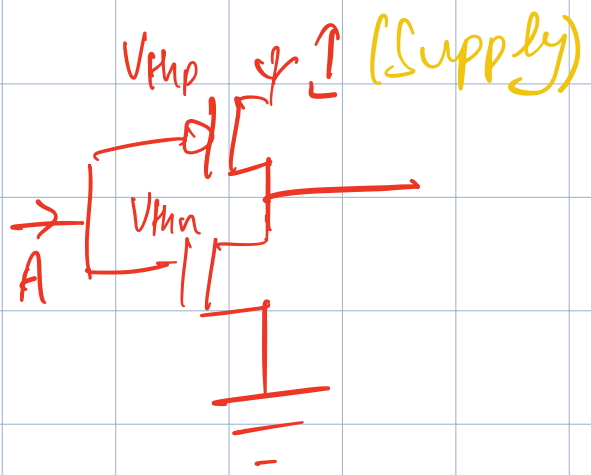


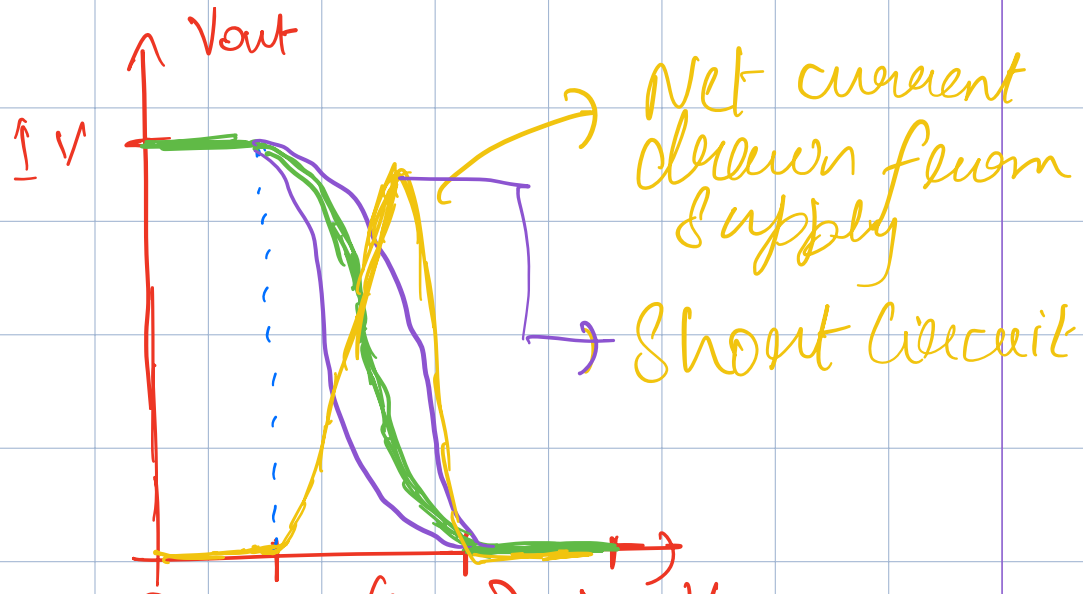


Non-ideal case :-

NMOS : On if $V_i > V_{th_n}$

PMOS : On if $V_i < V$

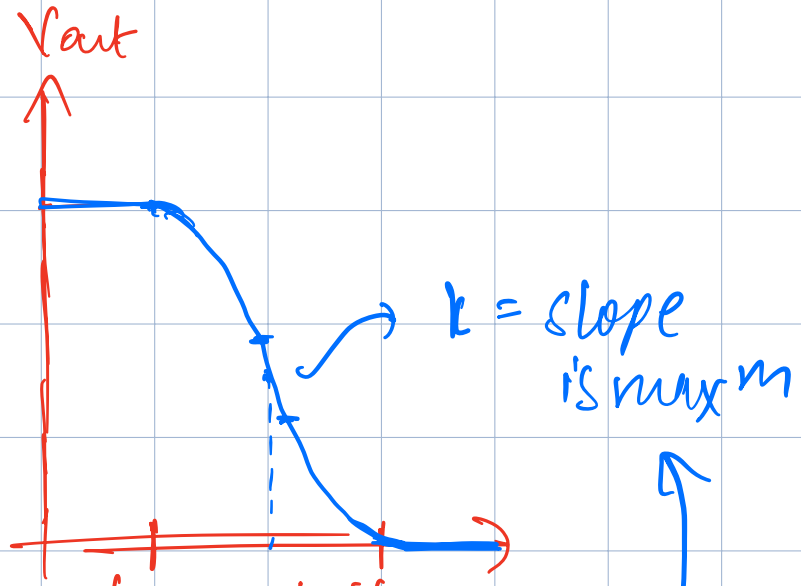




NMOS ON
PMOS off

NMOS still off,
PMOS still ON

NMOS ON,
PMOS also ON

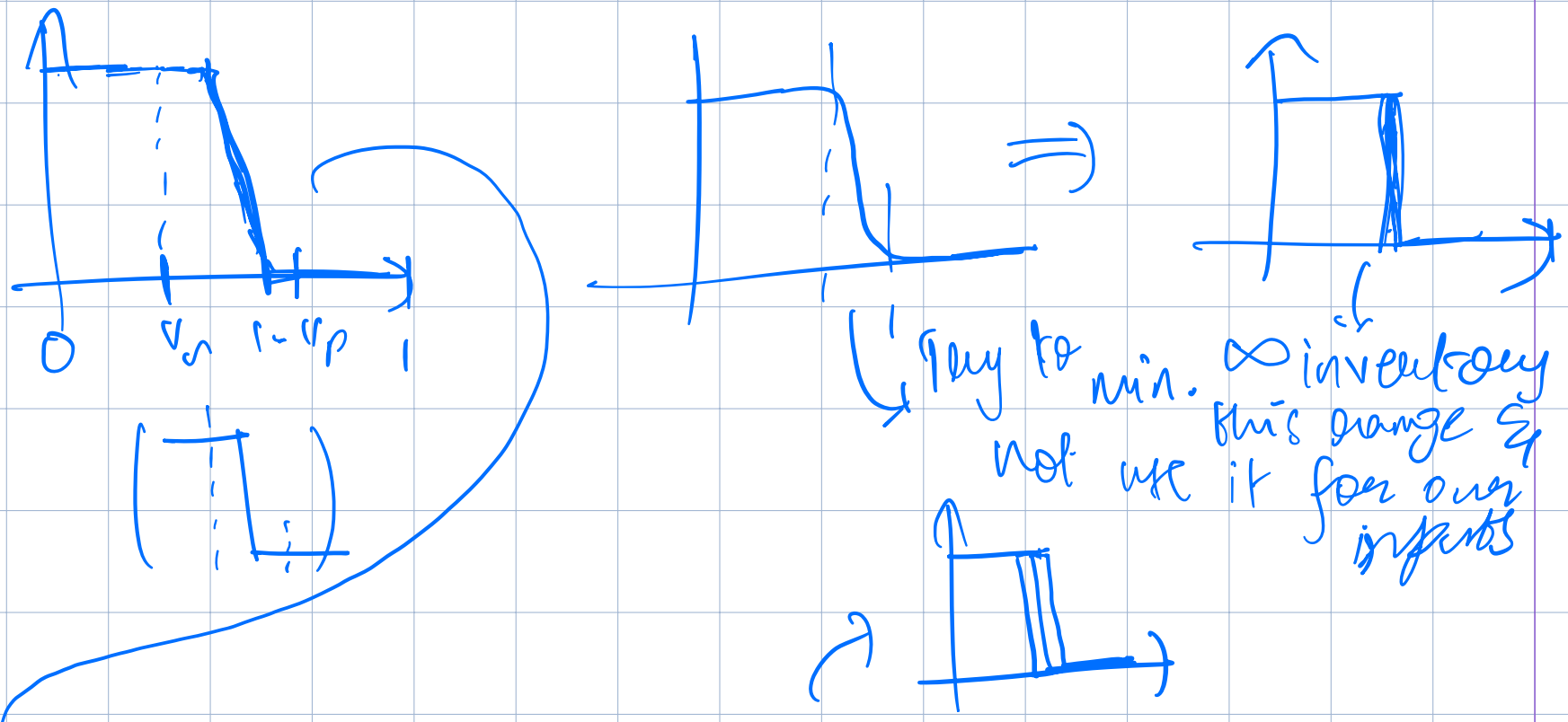


Amplifier

$k = \frac{\Delta V_{out}}{} \approx$ slope

ΔV_{in}

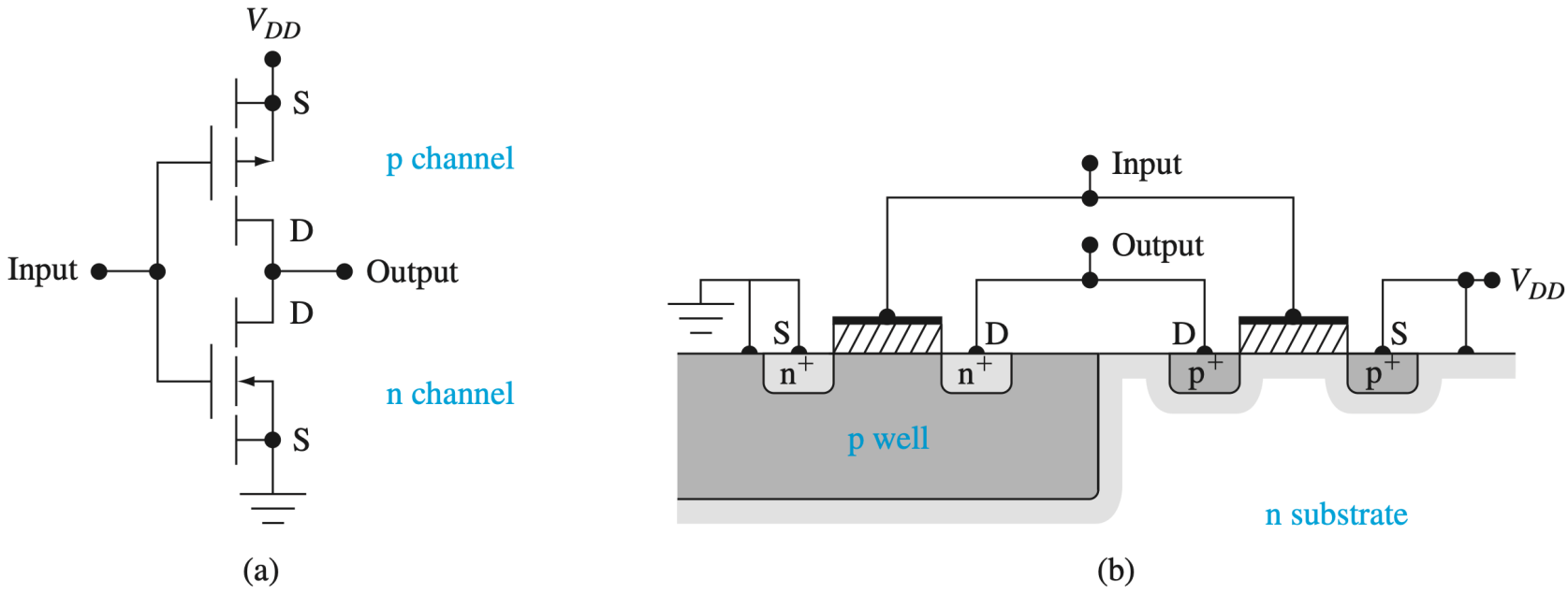
As no. of inverters ↑↑; it approaches logical 1 or 0
(odd. no.)



But, slopes are dependent on external conditions, like temperature.

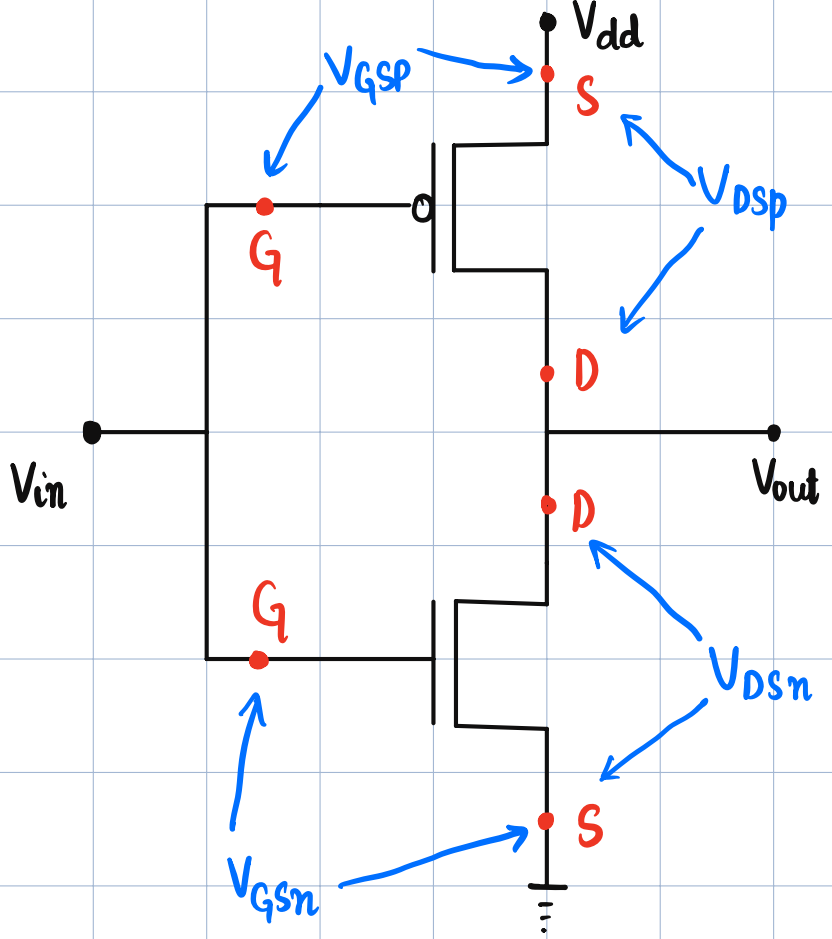
V_{DD} I_V (Source)

Grille
Fermée 0 V (Drain)



https://www.optima.ufam.edu.br/SemPhys/Downloads/Neamen.pdf

CMOS Inverter Voltage Transfer Characteristics



- $V_{Tn} > 0$, $V_{Tp} < 0$
- $V_{GSn} = (V_G - V_S)_n = V_{in}$
- $V_{DSn} = (V_D - V_S)_n = V_{out}$
- $V_{GSp} = (V_G - V_S)_p = V_{in} - V_{dd}$
- $V_{DSp} = (V_D - V_S)_p = V_{out} - V_{dd}$

nMOS

- $V_{GSn} < V_{Tn} \Rightarrow$ cutoff region
- $V_{GSn} > V_{Tn} \Rightarrow$ linear / saturation region.
- $V_{GSn} - V_{Tn} > V_{DSn} \Rightarrow$ linear

  $V_{GSn} - V_{Tn} < V_{DSn} \Rightarrow$ saturation

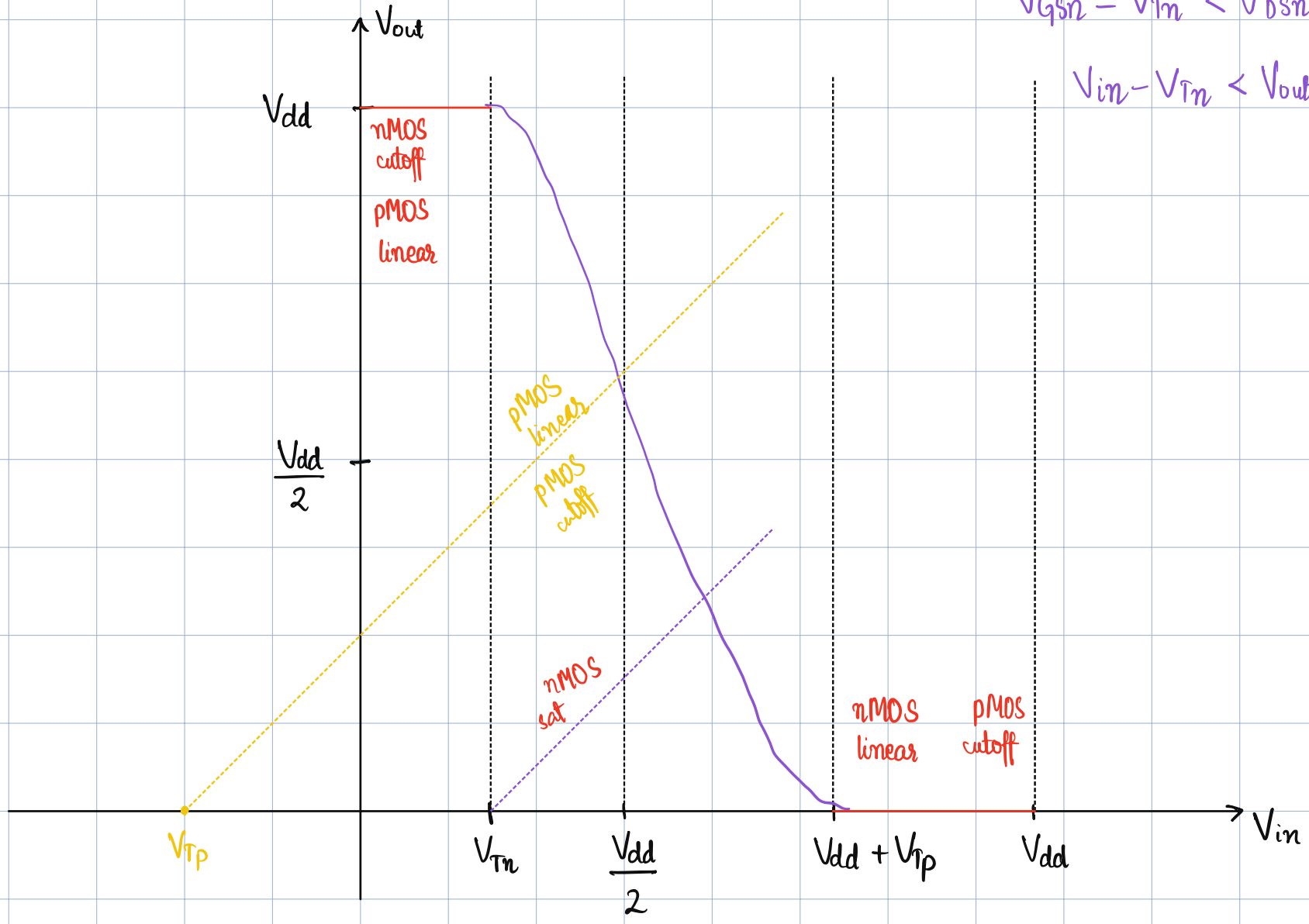
pMOS

- $V_{GSp} > V_{Tp} \Rightarrow$ cutoff region
- $V_{GSp} < V_{Tp} \Rightarrow$ linear / saturation region
- $V_{GSp} - V_{Tp} > V_{DSp} \Rightarrow$ saturation region

  $V_{GSp} - V_{Tp} < V_{DSp} \Rightarrow$ linear region

$V_{GSn} - V_{Tn} < V_{DSn}$

$V_{in} - V_{Tn} < V_{out}$



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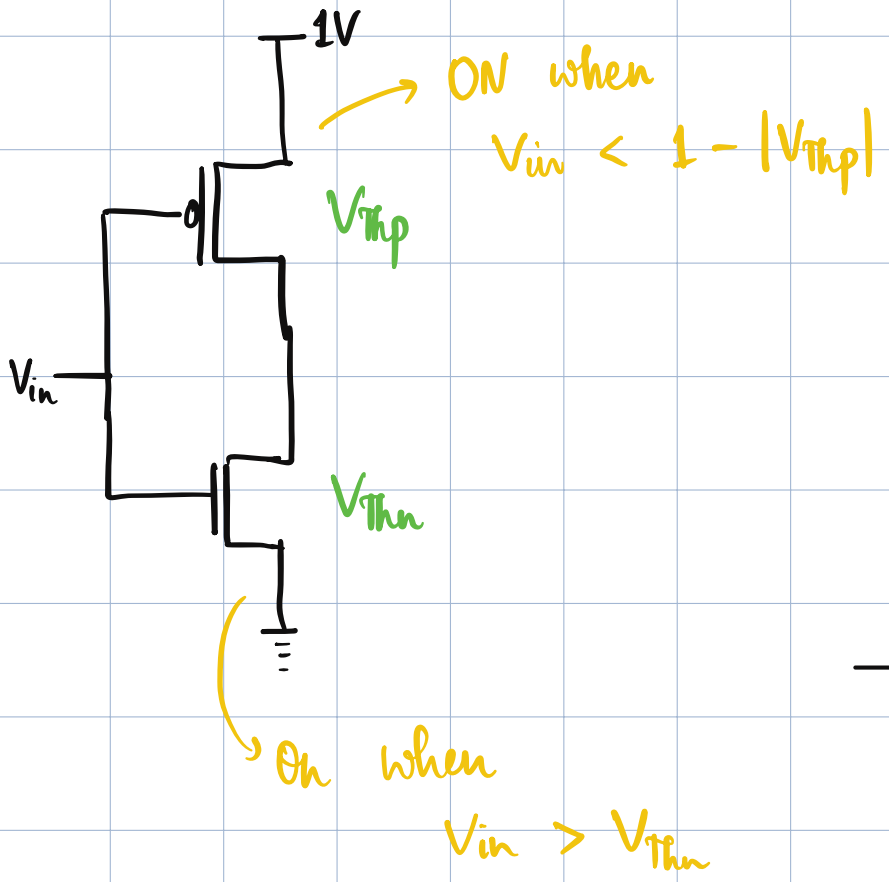
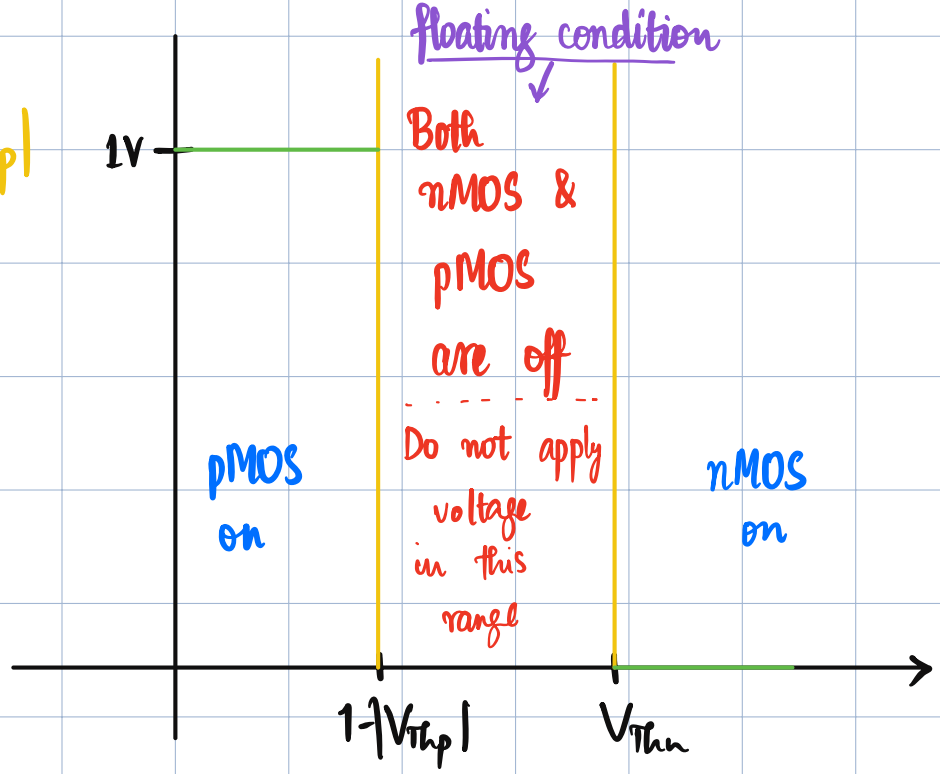
$V_{thn} > V_{dd} + V_{Thp}$ ($V_{dd} = 1$)

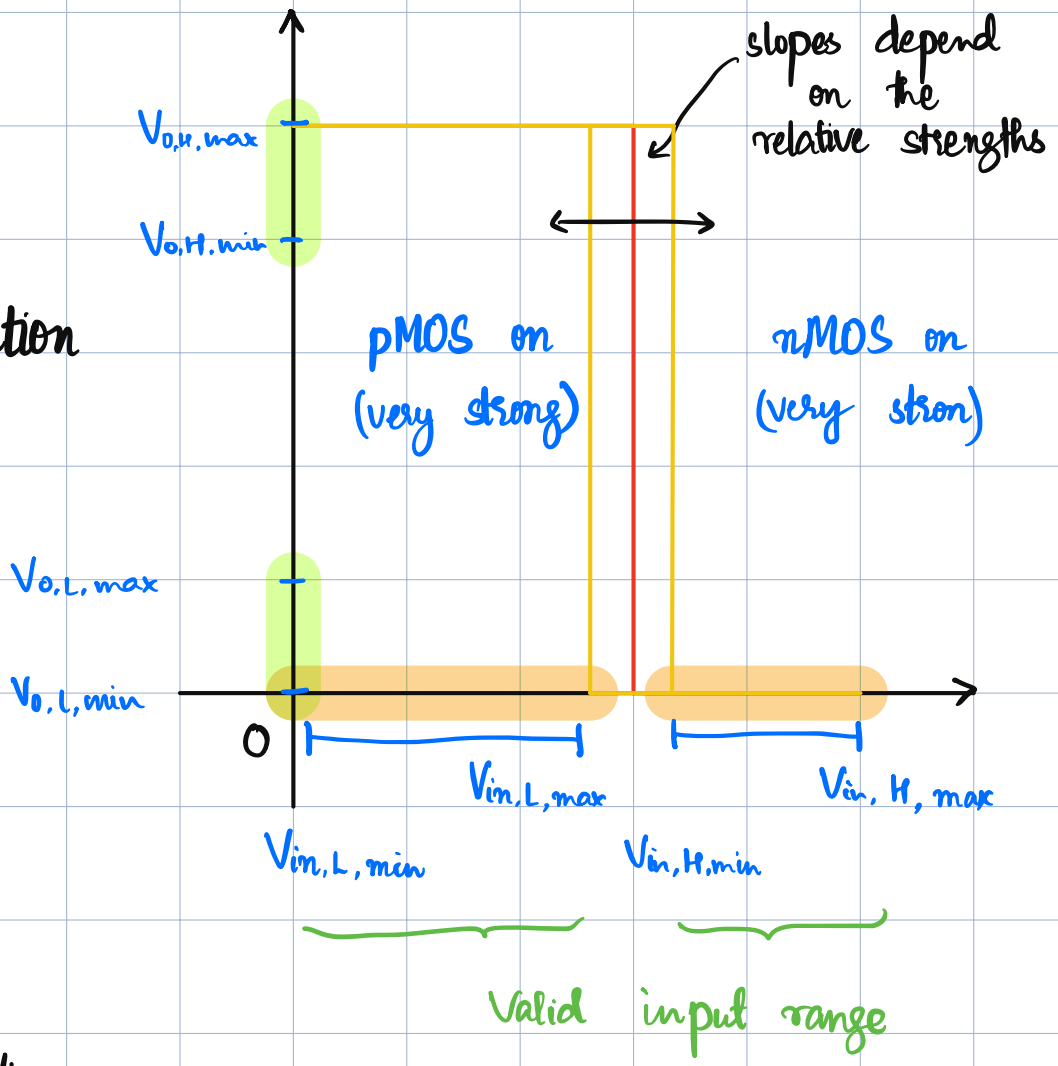
$1 - |V_{Thp}|$

Both threshold voltages are high

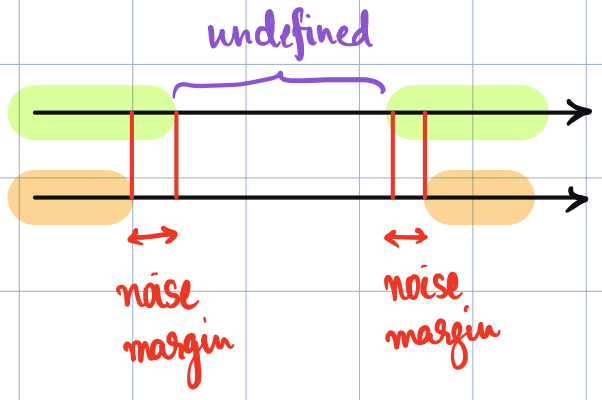




Change in characteristics due to P - V - T variation

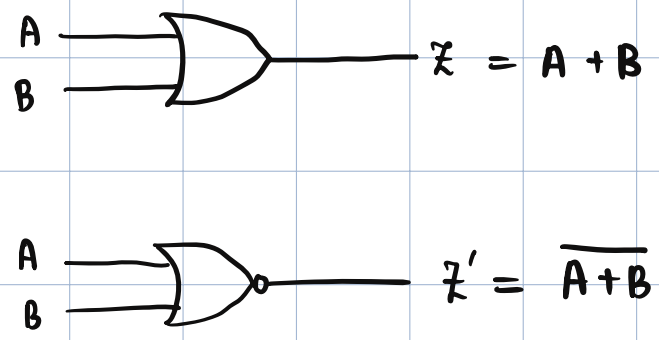


Input range should be a superset of output ranges



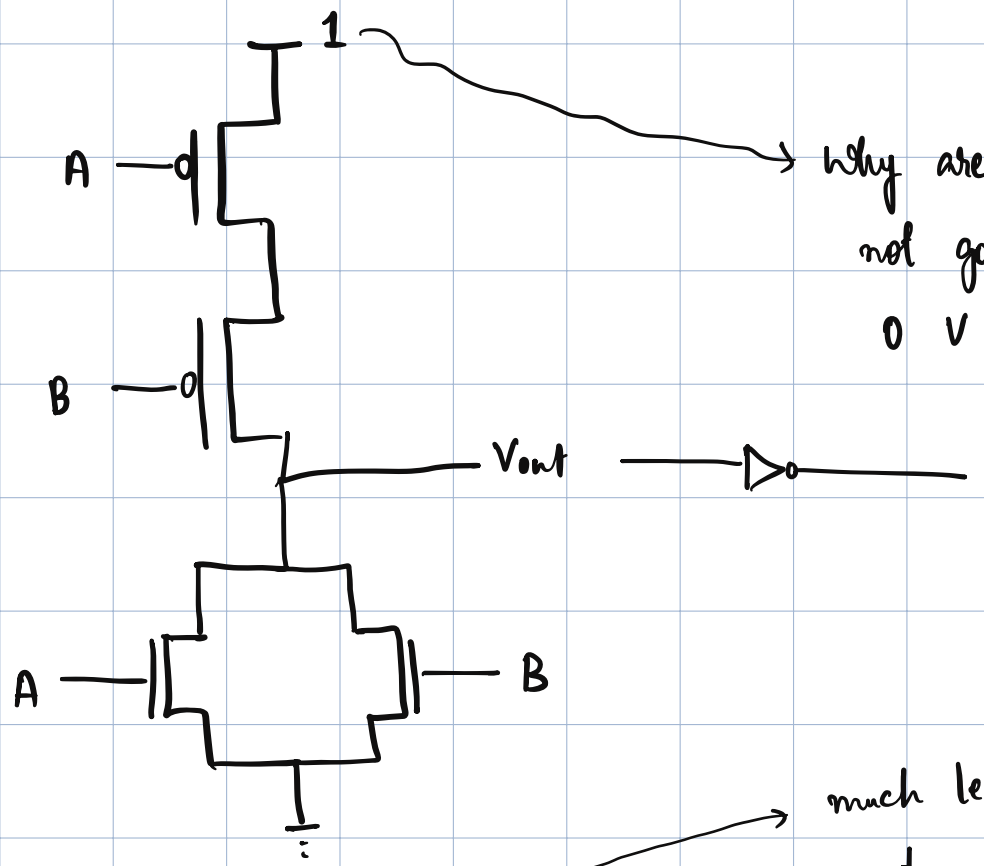
→ input for some other gate

OR / NOR Gate



A	B	Z = A+B	Z' = $\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

To implement NOR



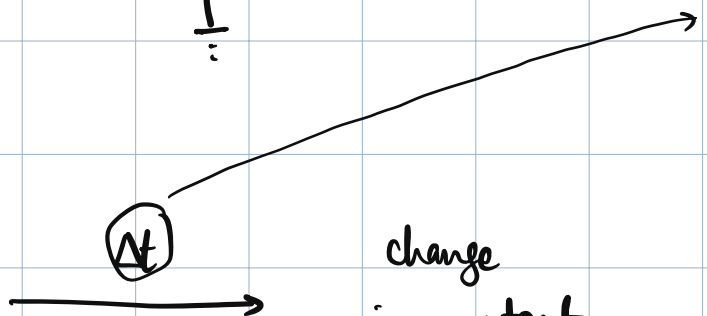
→ Why are pMOS not good for 0 V?

0, 0 → 1

0, 0 → 0 !

hard

Speed of gates

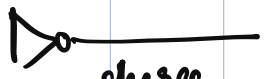


change in input voltage ΔV_{in}

change in output voltage ΔV_{out}

→ much less that t speed of light

even



charge accumulates,

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$$F(A, B, C, \ldots) = (A \cdot \overline{B} \cdot C + B \cdot \overline{C} \cdot D + E \cdot F) \cdot (\ldots)$$

literals

output variable

$$F(A, B, C) = Z$$

design a circuit for Z

↳ ① from basics → use nMOS pMOS

↳ ② use already available gates (NAND, NOR)

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$\rightarrow \overline{A} \cdot \overline{B} \cdot C$

+

$\rightarrow A \cdot \overline{B} \cdot \overline{C}$

+

$\rightarrow A \cdot B \cdot \overline{C}$

minterms

Analyse truth table row-by-row

→ Observe rows where we get 1 (Similar to how we did when designing NOR, NAND gate)

0 0 1 → 1

To get 1 : $\bar{A} \cdot \bar{B} \cdot C$

$\therefore \quad Z = \bar{A} \cdot \bar{B} \cdot C + A \cdot \bar{B} \cdot \bar{C} + A \cdot B \cdot \bar{C}$

	A	B	C	Z
m_0	0	0	0	0
m_1	0	0	1	1
m_2	0	1	0	0
m_3	0	1	1	0
m_4	1	0	0	1
m_5	1	0	1	0
m_6	1	1	0	1
m_7	1	1	1	0

$$F(A,B,C) = \bar{A}\cdot\bar{B}\cdot C + A\cdot\bar{B}\cdot\bar{C} + A\cdot B\cdot\bar{C}$$

$$= \sum(m_1, m_4, m_6)$$

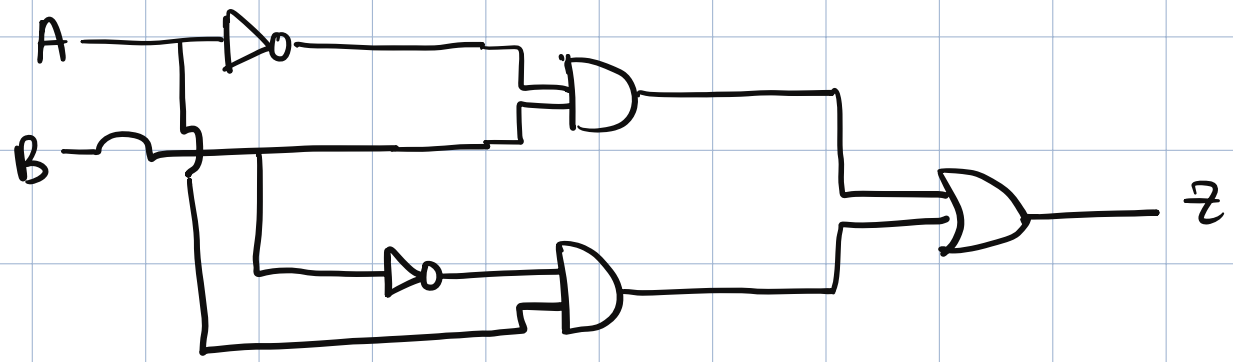
Sum of Products realisation (SoP)

Ex:- $F(A,B) = \sum(m_1, m_2)$

$m_1 \rightarrow \bar{A}\cdot B$ $\quad$ $m_2 \rightarrow A\cdot\bar{B}$

$$F(A,B) = \bar{A}\cdot B + A\cdot\bar{B}$$

	A	B	Z
m_0	0	0	0
m_1	0	1	1
m_2	1	0	1
m_3	1	1	0



less 0s more 1s

	A	B	C	Z	
m_0	0	0	0	1	M_0
m_1	0	0	1	0	M_1
m_2	0	1	0	1	M_2
m_3	0	1	1	1	M_3
m_4	1	0	0	0	M_4
m_5	1	0	1	1	M_5
m_6	1	1	0	1	M_6
m_7	1	1	1	0	M_7

$$F(A,B,C) = Z$$

$$\overline{Z} = \sum(m_1, m_4, m_7)$$

$$= \overline{A}\cdot\overline{B}\cdot C + A\cdot\overline{B}\cdot\overline{C} + A\cdot B\cdot C$$

$$Z = \bar{\bar{Z}} = \left(\bar{A}\cdot\bar{B}\cdot C + A\cdot\bar{B}\cdot\bar{C} + A\cdot B\cdot C\right)'$$

$$= \left(\overline{\bar{A}\cdot\bar{B}\cdot C}\right)\cdot\left(\overline{A\cdot\bar{B}\cdot\bar{C}}\right)\cdot\left(\overline{A\cdot B\cdot C}\right)$$

$$= \underbrace{(A + B + \bar{C})\cdot(\bar{A} + B + C)\cdot(\bar{A} + \bar{B} + \bar{C})}$$

Product of Sum realization (POS)

maxterm } by default 1

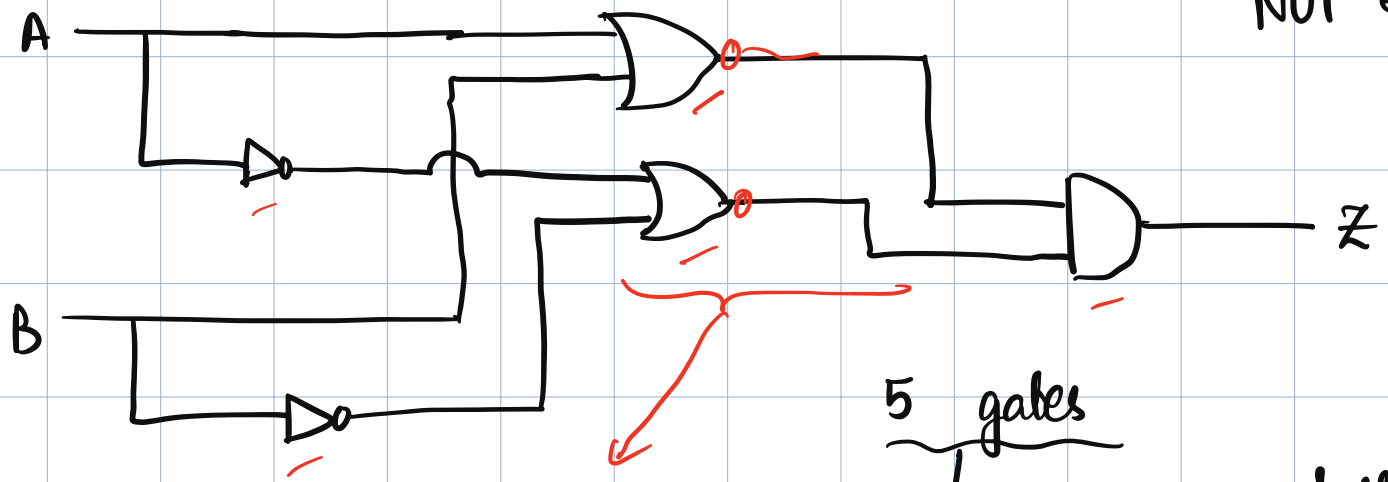
$$\therefore F(A, B, C) = \Pi(M_1, M_4, M_7)$$

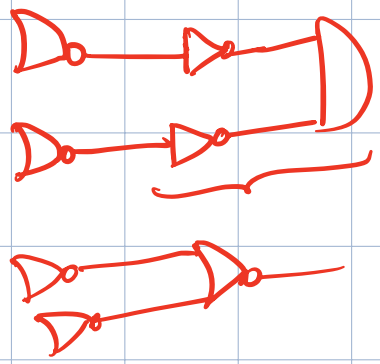
E.g: $F(A, B) = \Pi(M_0, M_3)$

$$F(A \cdot B) = (A + B) \cdot (\bar{A} + \bar{B})$$

A	B	Z	
0	0	0	M_0
0	1	1	M_1
1	0	1	M_2
1	1	0	M_3

NOT equal operator





5 gates

how can we reduce the number of gates