2024/08/12

$A \cdot B + \bar{A} \cdot C + (B \cdot C)$ → can be ignored

$= A \cdot B + \bar{A} \cdot C + B \cdot C \cdot (A + \bar{A})$

$= A \cdot B + \bar{A} \cdot C + B \cdot C \cdot A + B \cdot C \cdot \bar{A}$

$= A \cdot B \cdot (1 + C) + \bar{A} \cdot C \,(1 + B)$

$= AB + \bar{A} \cdot C$ } Consensus theorem

dual :

$(A + B) \cdot (\bar{A} + C) \cdot (B + C) = (A + B) \cdot (\bar{A} + C)$

Logical Operators

i) $Z = \bar{A}$ → 'NOT' operation

↑ Complement of A

truth table of NOT

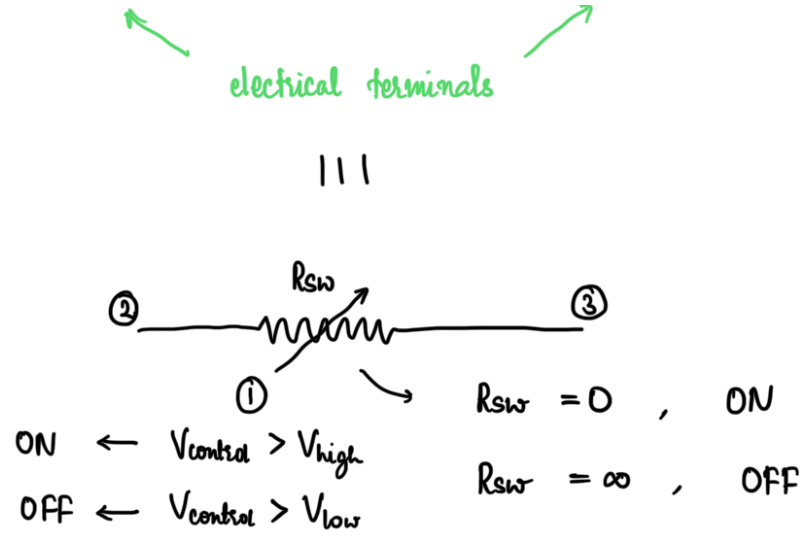
A	Z
0	1
1	0

circuits can be implemented using logical operations

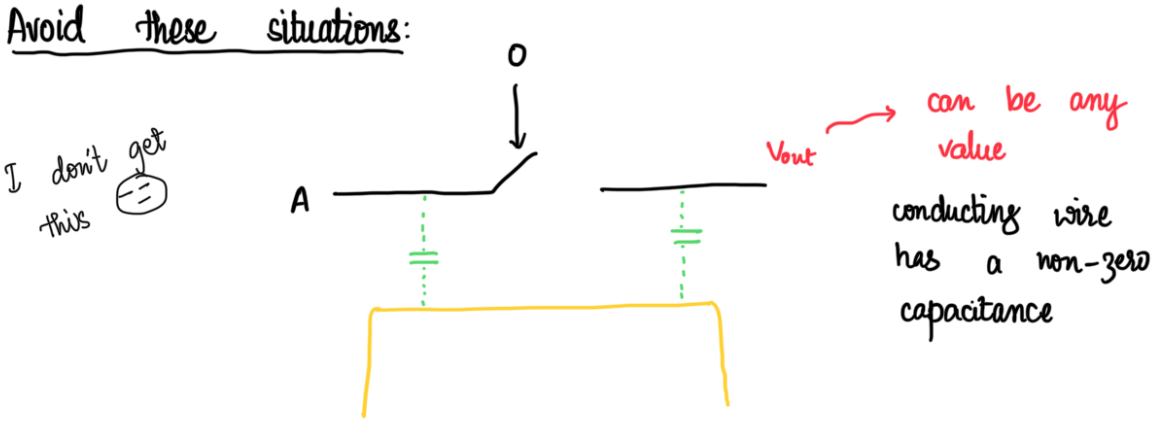
NOT gate ⇝ can be very easily implemented using switches

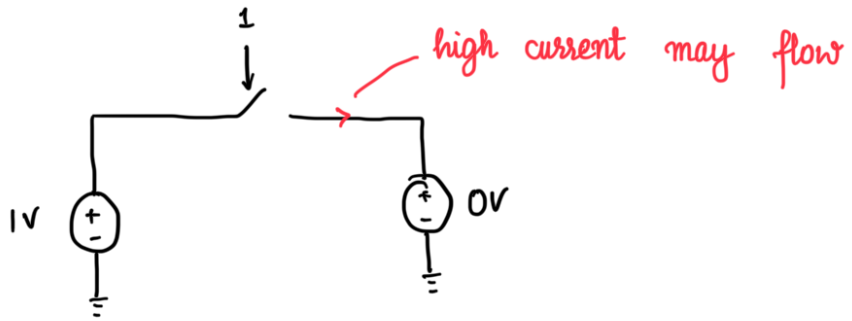
Switch :- electrical device that has two states

} what exactly does this mean?

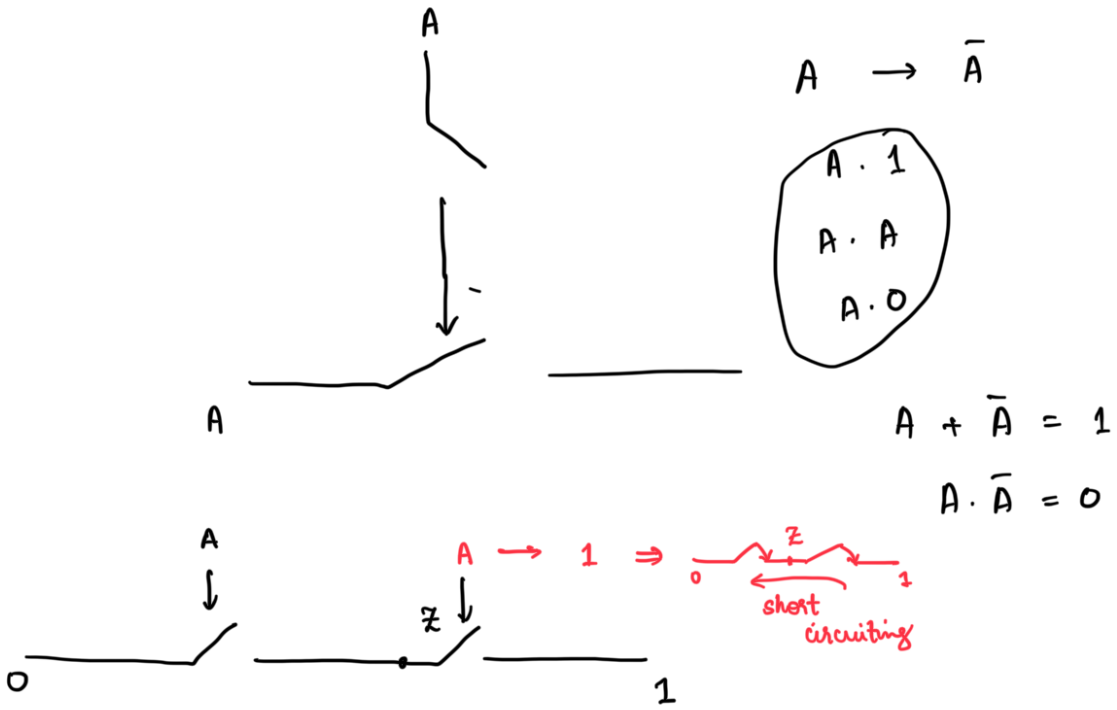


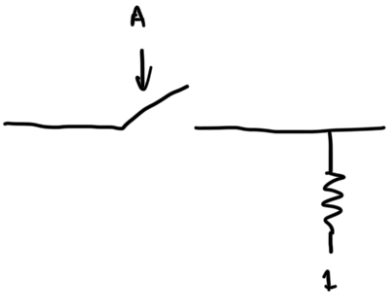
How to implement a not gate?

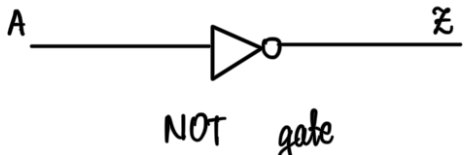




Low impedance nodes, full floating nodes



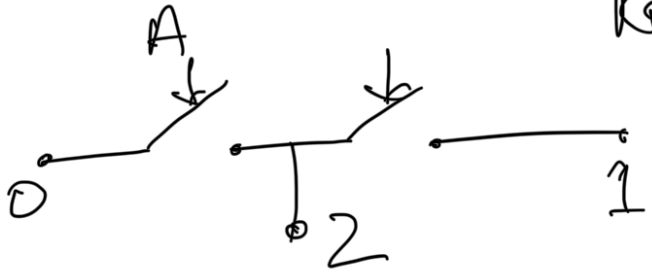




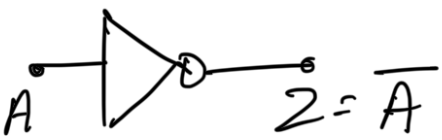
NOT gate

Roshan's Notes

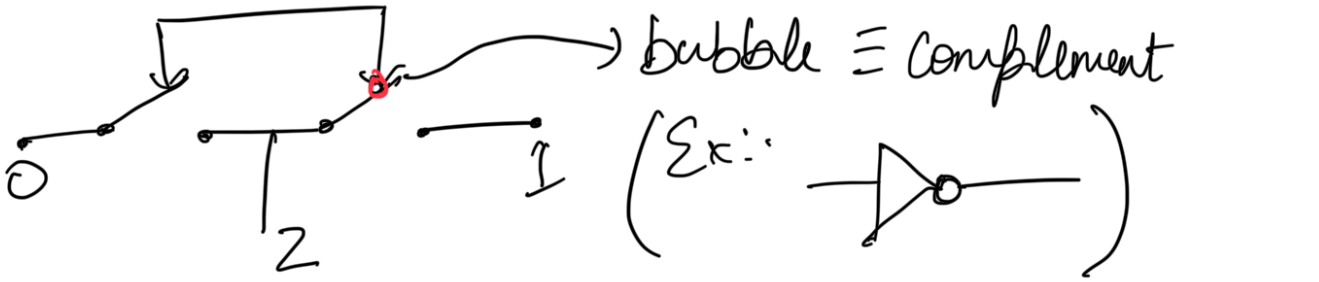
2024|08|14

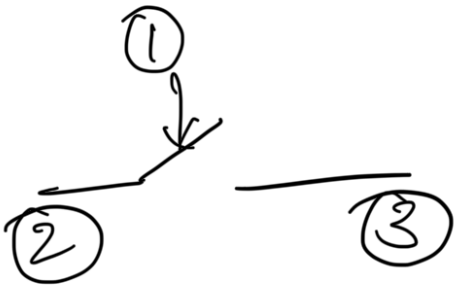


NOT Gate :-



① Vcontrol





Electronic vs Electrical

electronic ⊆ electrical

Some non-conductor in circuit, like semi-conductor

Easier to control semi-conductors' properties (/ or 0) than conductors

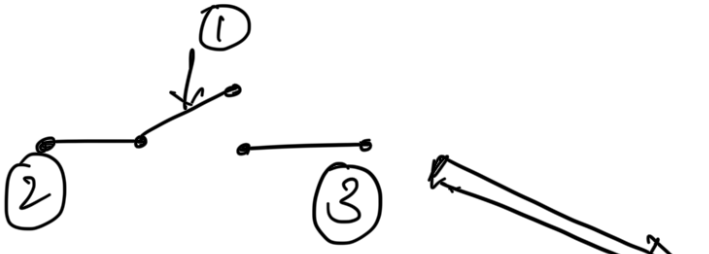
SOLID STATE PHYSICS

No mechanical movement / relays

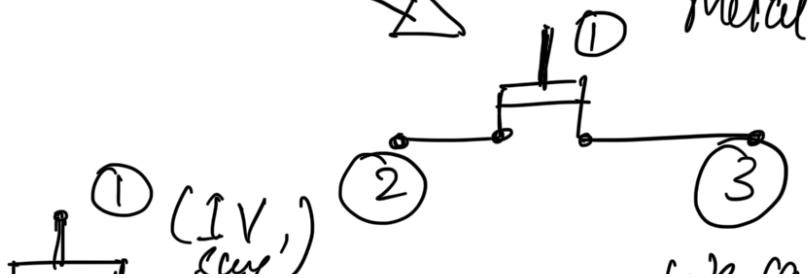
* Effectively Implemented using FIELD EFFECT TRANSISTORS (FET)

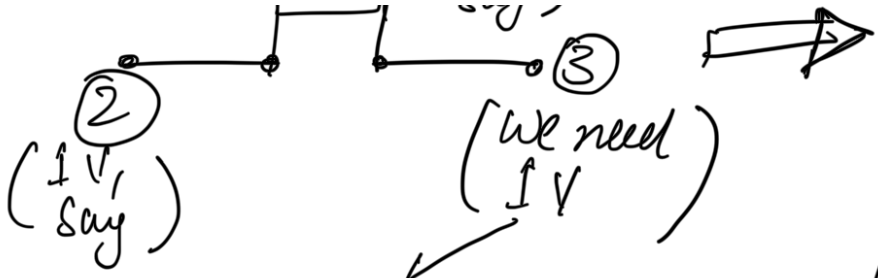
MOSFET

metal Oxide Semi-conductor



Ex:-





we control pass high voltage from terminal 2 to 3.

But 0V is possible

Not (1V) technically

Binary → 0V (low)

→ 1V (means high voltage)

* If relative voltage difference across FET ↑↑; its conductivity ↑↑ (How?)

↳ **Enhancement Mode Devices**

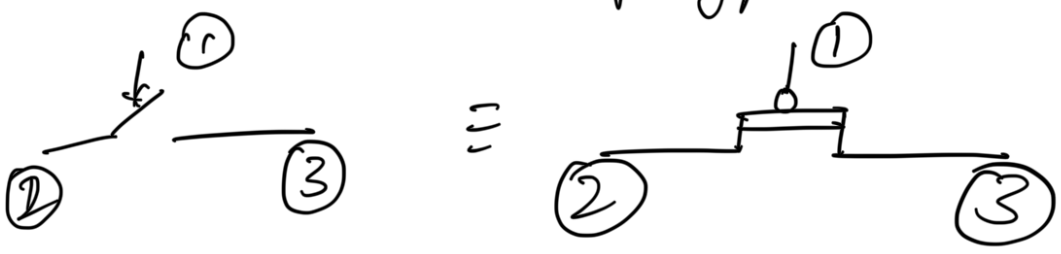
ON iff $V_{1-2,3} > V_{th}$ → Threshold

OFF iff $V_{1-2,3} < V_{th}$

In ON side, N-MOSFET can only pass low voltage ↳ n-type semiconductor

2nd Type : PMOS

↳ p-type semiconductor:-



ON iff $V_{1-2,3} < V_{th}$

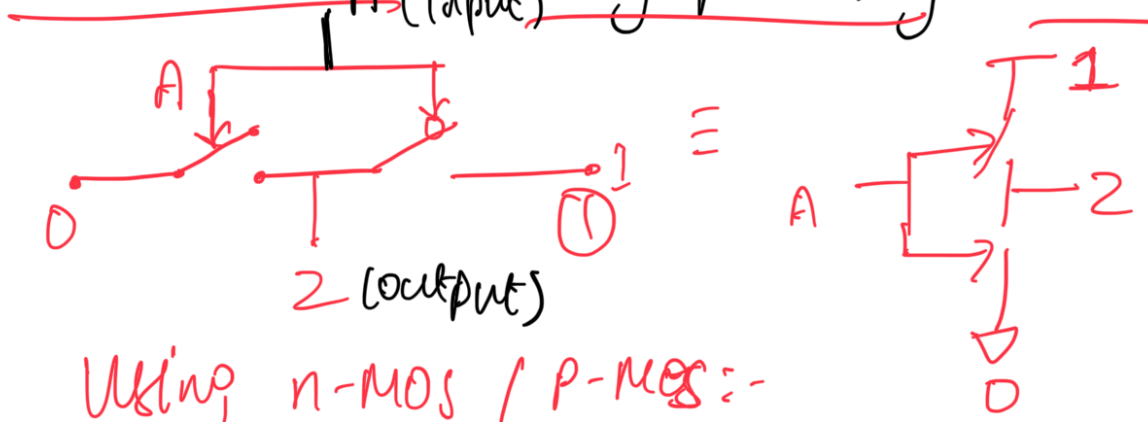
OFF iff $V_{1-2,3} > V_{th}$

Note :-

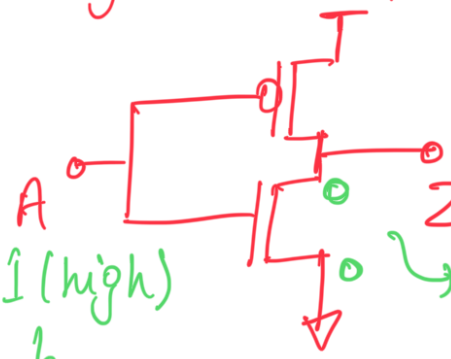
V_{th} is always

a -ve number

($V_{t-2,3}$, $V_{GS} < 0$) In ON side, PMOS can only pass high voltage



Using n-MOS / p-MOS :-



$(\because 2 = \bar{A})$

If 1 (high) → ∵ n-mos transfers low voltage

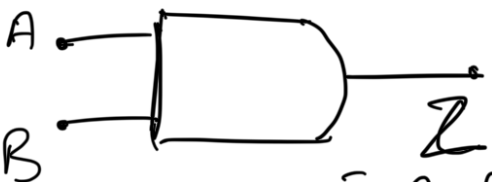
↳ Similarly, we can show for A = 0 (low)

↳ Complementary MOS Technology ($\because$ 1 p-MOS, 1 n-MOS)

(For same dimensions, p-MOS is 3x less conductive than n-MOS)

CMOS chip in CPU (date & time)

AND GATE :-



A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

$= A \cdot B$

TRY to implement AND gate using.